

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2012-02-15

SCHEM,MLB_KEPLER_2PHASE,J31

FRB & RISK RAMP 02/15/12

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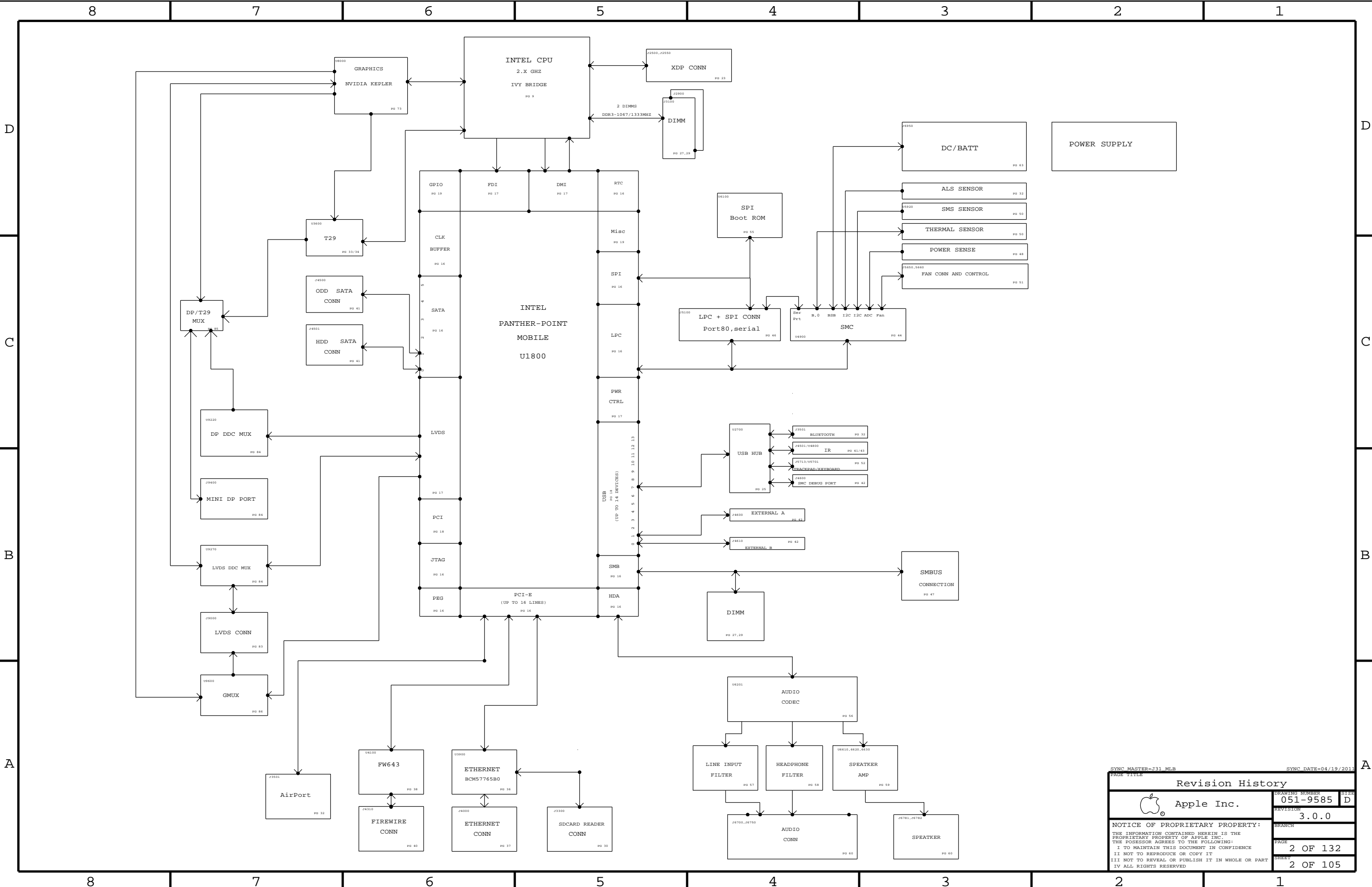
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Schematic / PCB #'s

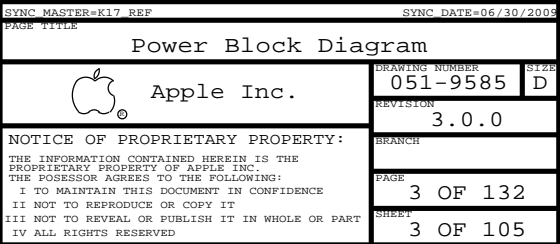
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820-3330	1	PCBF,MLB_KEPLER_2PHASE,J31	PCB	CRITICAL	

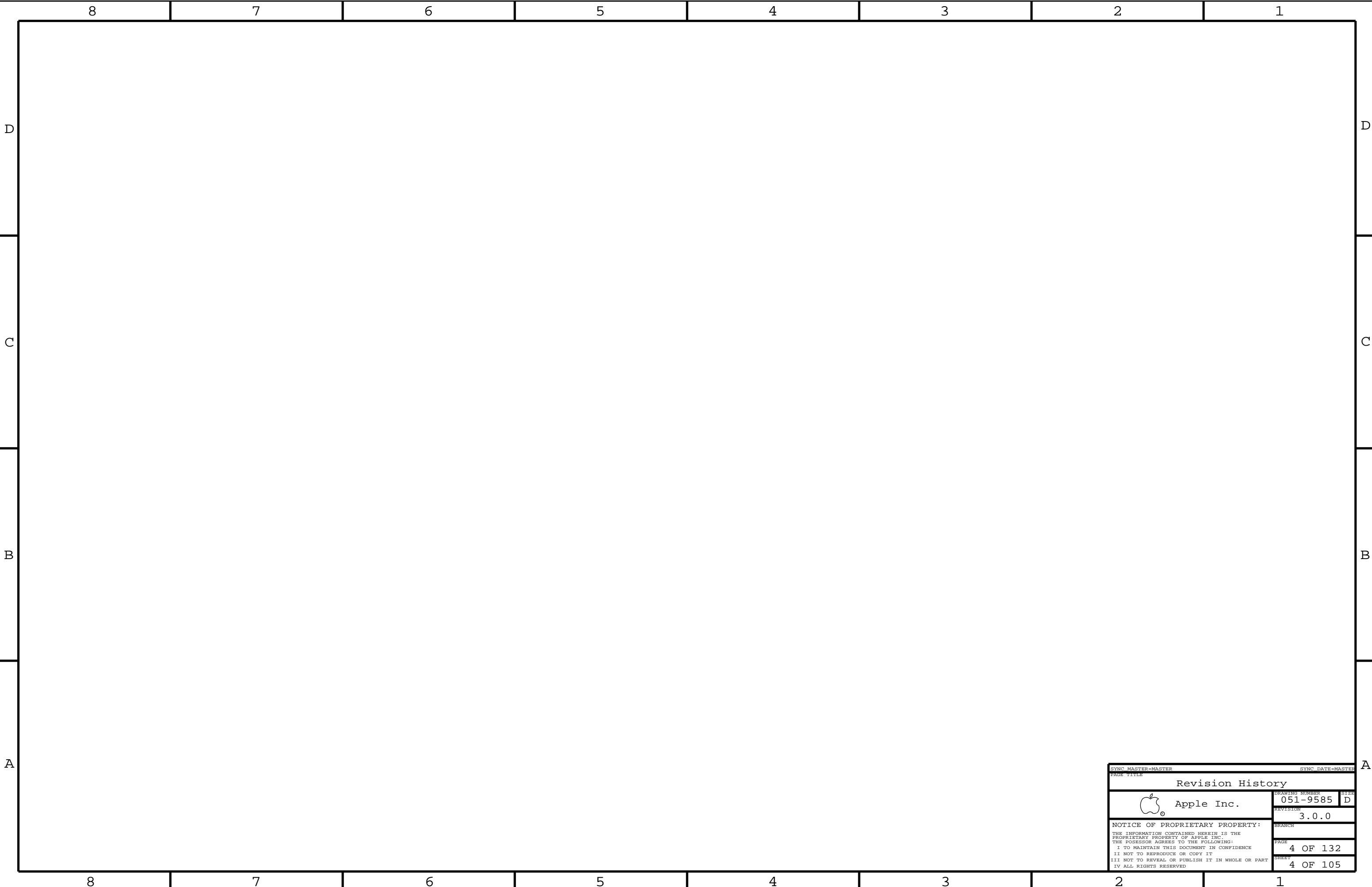
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LAST_MODIFIED=Wed Feb 15 20:30:03 2012

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		3.0.0		
		BRANCH		
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SYNC MASTER=MASTER

SYNC DATE=MASTER

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SIZE
D

BOM VARIANTS - FSB

Bar Code Labels / EEEE #'s					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F327]	CRITICAL	EEEE:F327
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F32C]	CRITICAL	EEEE:F32C
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F325]	CRITICAL	EEEE:F325
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F324]	CRITICAL	EEEE:F324
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F328]	CRITICAL	EEEE:F328
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F329]	CRITICAL	EEEE:F329

SUB BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F327]	CRITICAL	EEEE:F327
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F32C]	CRITICAL	EEEE:F32C
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F325]	CRITICAL	EEEE:F325
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F324]	CRITICAL	EEEE:F324
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F328]	CRITICAL	EEEE:F328
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_F329]	CRITICAL	EEEE:F329

BOM GROUPS

REF	DES	COMMENTS:
		Programmables - All Builds

Alternate Parts

PSOC

341S2830	1	IC_OHLD_LATTICE_OHMS_631/63P_331	U9600	CRITICAL	OHMS_PROG
336S0042	1	IC_PAB_LATTICE_LPWFS-SE-9_132 ANAL OSMON	U9600	CRITICAL	OHMS_BLANK
341S2384	1	IR_BROOKS_11_CVCK3433-LPWC	U4800	CRITICAL	IR_PROG
341S3430	1	IC_T29_KEROMON_LB_030/031	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC_KEROMON_0003AL_B09_0003	U3690	CRITICAL	T29ROM:BLANK
341S3365	1	IC_PROGRAMM_LP0111A_T29_P00T_MCU_P77_000P003_331	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC_MCU_32B_LP0111A_1609_ZER_000P025	U9330	CRITICAL	T29MCU:BLANK
335S0852	1	IC_GPUSROM_331_B1ANK	U8701	CRITICAL	GPUSROM:BLANK

ETHERNET ROM

Module Parts

5FI ROMPD Parts

SYNC MASTER=K17 REF SYNC DATE=05/28/2009

BOM Configuration



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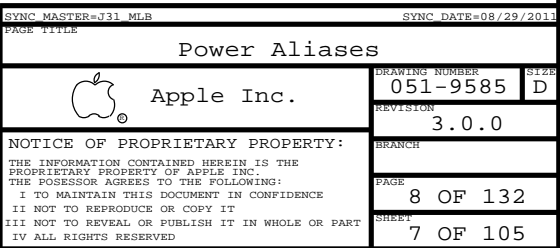
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REVISION		

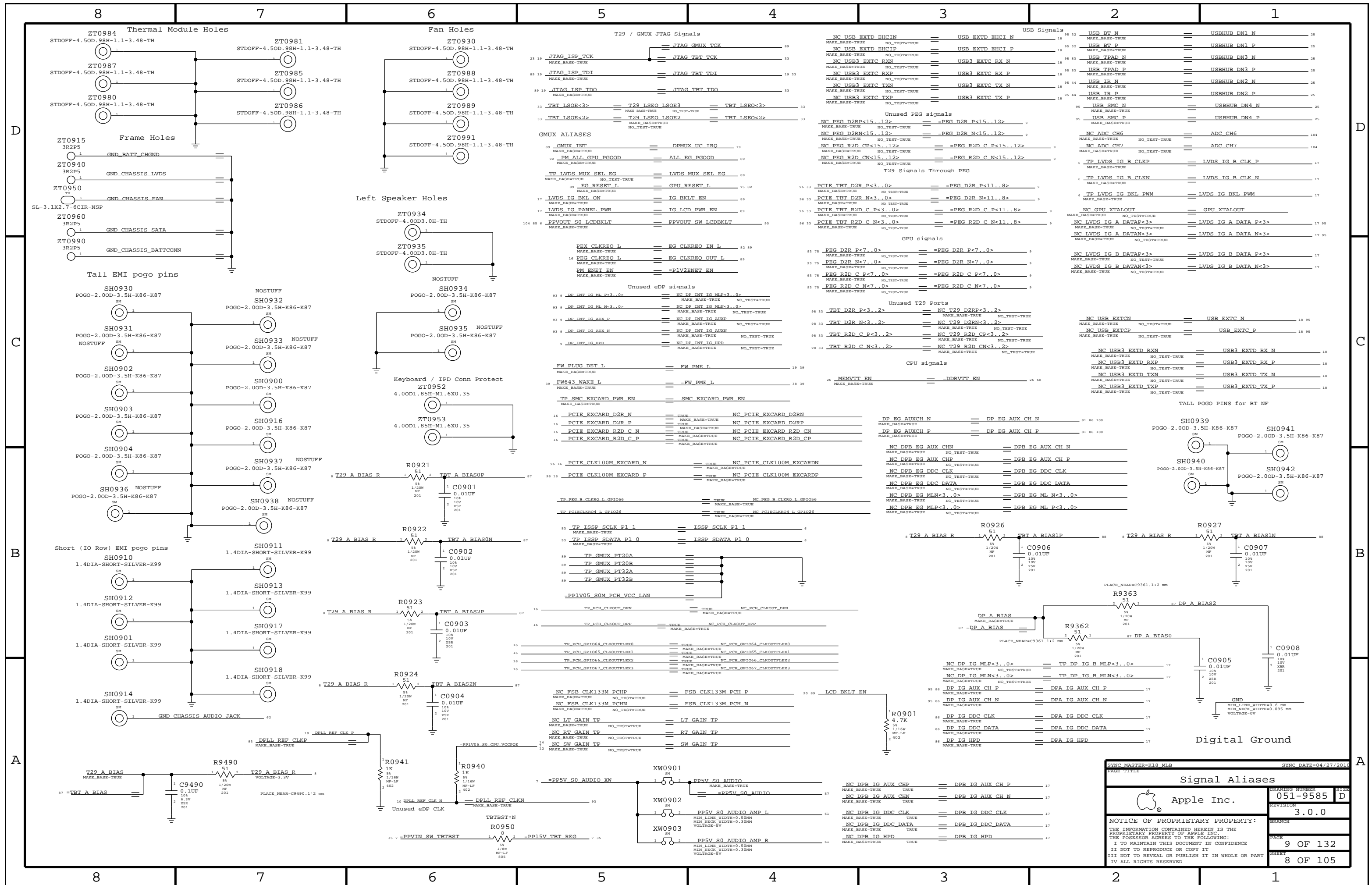
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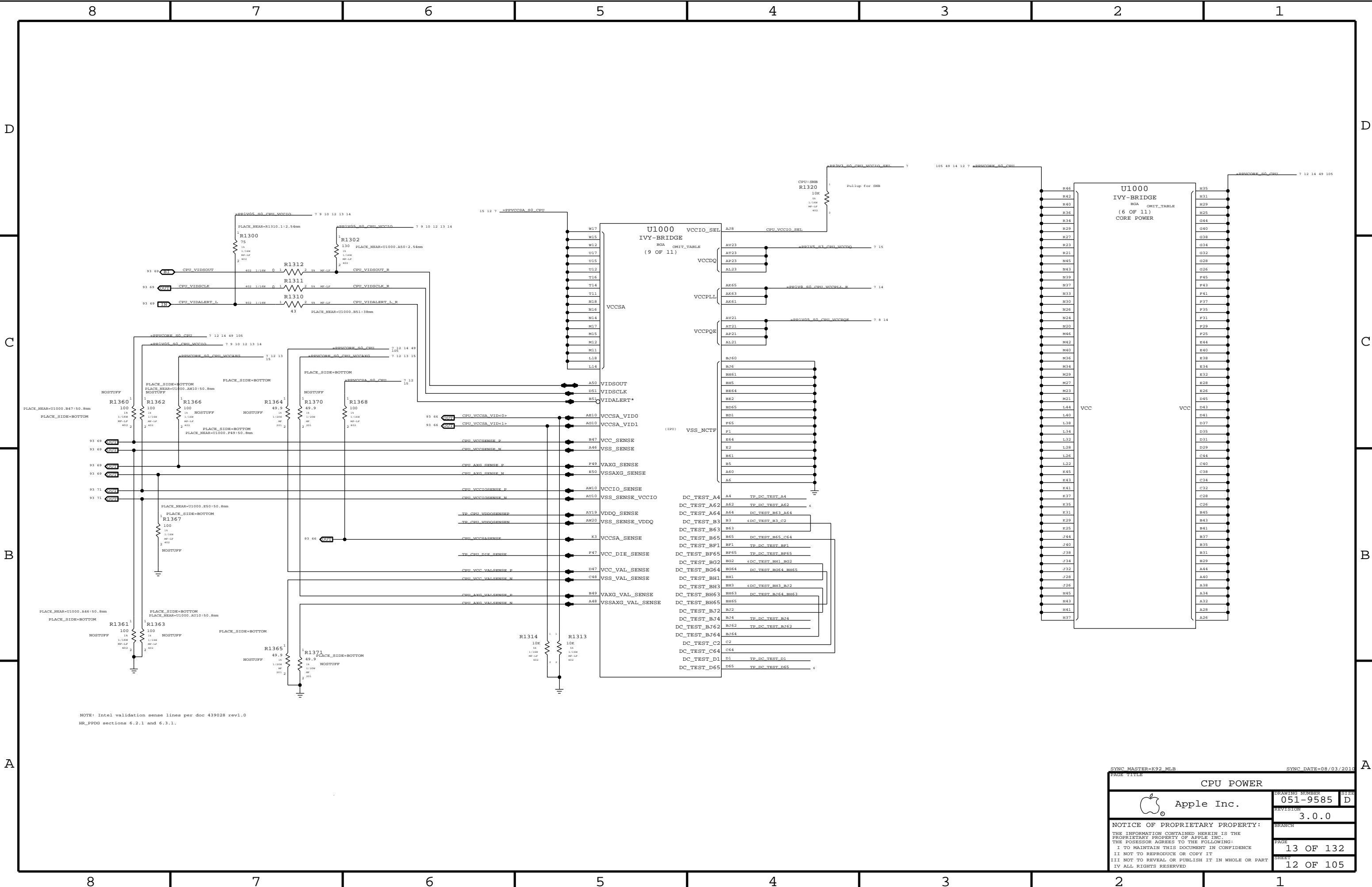
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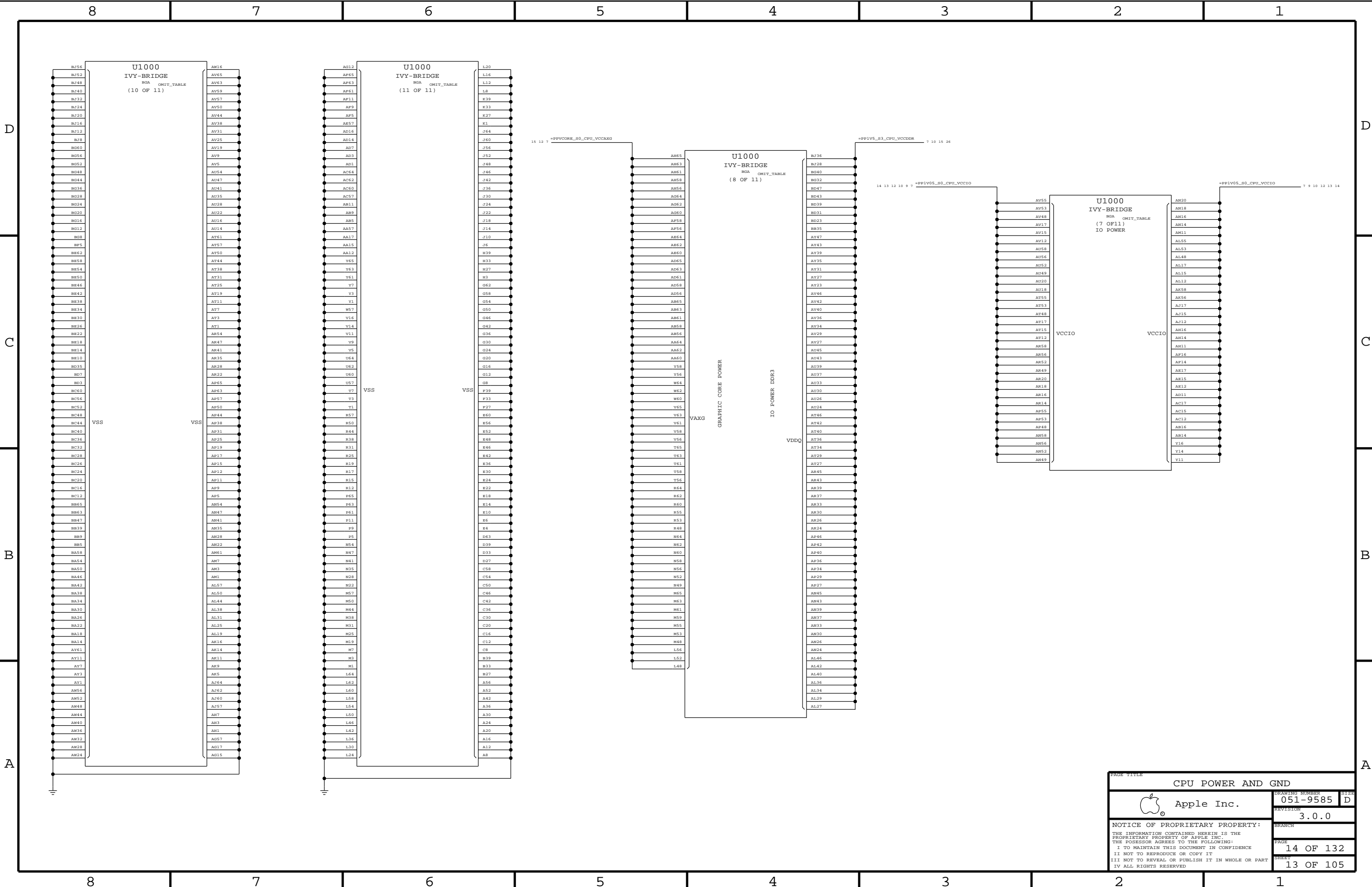
8	7	6	5	4	3	2	1
Functional Test Points				ICT Test Points			
J5650 (LEFT FAN CONN)				CPU NO_TESTS			
FUNC_TEST				NO_TEST			
PP5V_S0				TP CPU RSVD<65..62>			
FAN LT_PWM				TP CPU RSVD<58..45>			
FAN LT_TACH				TP CPU RSVD<43..32>			
GND				TP CPU RSVD<27..26>			
J5660 (RIGHT FAN CONN)				TP CPU RSVD<24..15>			
PP5V_S0				TP CPU RSVD<2..1>			
FAN RT_PWM				TP CPU RSVD NCTP<8..5>			
FAN RT_TACH				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J6780 (MIC CONN)				TP CPU RSVD NCTP<8..5>			
BI_MIC_N				TP CPU RSVD NCTP<8..5>			
BI_MIC_SHIELD				TP CPU RSVD NCTP<8..5>			
BI_MIC_P				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J3501 & J3502 (AIRPORT/BT/CAMERA CONN)				TP CPU RSVD NCTP<8..5>			
PCIE AP_R2D_P				TP CPU RSVD NCTP<8..5>			
PCIE AP_R2D_N				TP CPU RSVD NCTP<8..5>			
PCIE CLK100M AP_CONN_P				TP CPU RSVD NCTP<8..5>			
PCIE CLK100M AP_CONN_N				TP CPU RSVD NCTP<8..5>			
AP_CLKREQ_O_L				TP CPU RSVD NCTP<8..5>			
PCIE_WAKE_L				TP CPU RSVD NCTP<8..5>			
WIFI_EVENT_L				TP CPU RSVD NCTP<8..5>			
AP_RESET_CONN_L				TP CPU RSVD NCTP<8..5>			
PP3V3_WLAN				TP CPU RSVD NCTP<8..5>			
PP5V_S3_ALSCAMERA_F				TP CPU RSVD NCTP<8..5>			
SMBUS_SMC_2_S3_SDA				TP CPU RSVD NCTP<8..5>			
SMBUS_SMC_2_S3_SCL				TP CPU RSVD NCTP<8..5>			
USB_CAMERA_CONN_P				TP CPU RSVD NCTP<8..5>			
USB_CAMERA_CONN_N				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J5100				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
PP5V_S0				TP CPU RSVD NCTP<8..5>			
PP3V42_G3H				TP CPU RSVD NCTP<8..5>			
J6781 & J6782 (SPEAKERS CONN)				TP CPU RSVD NCTP<8..5>			
SPKRCONN_L_OUT_P				TP CPU RSVD NCTP<8..5>			
SPKRCONN_L_OUT_N				TP CPU RSVD NCTP<8..5>			
SPKRCONN_R_OUT_P				TP CPU RSVD NCTP<8..5>			
SPKRCONN_R_OUT_N				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J9000 (LVDS CONN)				TP CPU RSVD NCTP<8..5>			
PP3V3_SW_LCD				TP CPU RSVD NCTP<8..5>			
PP3V3_S0				TP CPU RSVD NCTP<8..5>			
PPVOUT_S0_LCDBKLT				TP CPU RSVD NCTP<8..5>			
LVDS_KMC_CLK				TP CPU RSVD NCTP<8..5>			
LVDS_KMC_DATA				TP CPU RSVD NCTP<8..5>			
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LVDS_CONN_B_CLK_F_P				TP CPU RSVD NCTP<8..5>			
LVDS_CONN_B_CLK_F_N				TP CPU RSVD NCTP<8..5>			
LED_RETURN_1				TP CPU RSVD NCTP<8..5>			
LED_RETURN_2				TP CPU RSVD NCTP<8..5>			
LED_RETURN_3				TP CPU RSVD NCTP<8..5>			
LED_RETURN_4				TP CPU RSVD NCTP<8..5>			
LED_RETURN_5				TP CPU RSVD NCTP<8..5>			
LED_RETURN_6				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J4500 (SATA ODD CONN)				TP CPU RSVD NCTP<8..5>			
PP5V_SW_ODD				TP CPU RSVD NCTP<8..5>			
SMC_ODD_DETECT				TP CPU RSVD NCTP<8..5>			
SATA_ODD_D2R_C_P				TP CPU RSVD NCTP<8..5>			
SATA_ODD_D2R_C_N				TP CPU RSVD NCTP<8..5>			
SATA_ODD_R2D_P				TP CPU RSVD NCTP<8..5>			
SATA_ODD_R2D_N				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J4501 (SATA HDD CONN)				TP CPU RSVD NCTP<8..5>			
PP5V_S0_HDD_FLT				TP CPU RSVD NCTP<8..5>			
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SATA_HDD_D2R_C_P				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J5815 (KBD BACKLIGHT CONN)				TP CPU RSVD NCTP<8..5>			
KBD_LED_ANODE				TP CPU RSVD NCTP<8..5>			
SMC_KBDLED_PRESENT_L				TP CPU RSVD NCTP<8..5>			
GND				TP CPU RSVD NCTP<8..5>			
J5713 (KEY BOARD CONN)				TP CPU RSVD NCTP<8..5>			
PP3V3_S4				TP CPU RSVD NCTP<8..5>			
PP3V42_G3H				TP CPU RSVD NCTP<8..5>			
WS_KBD1				TP CPU RSVD NCTP<8..5>			
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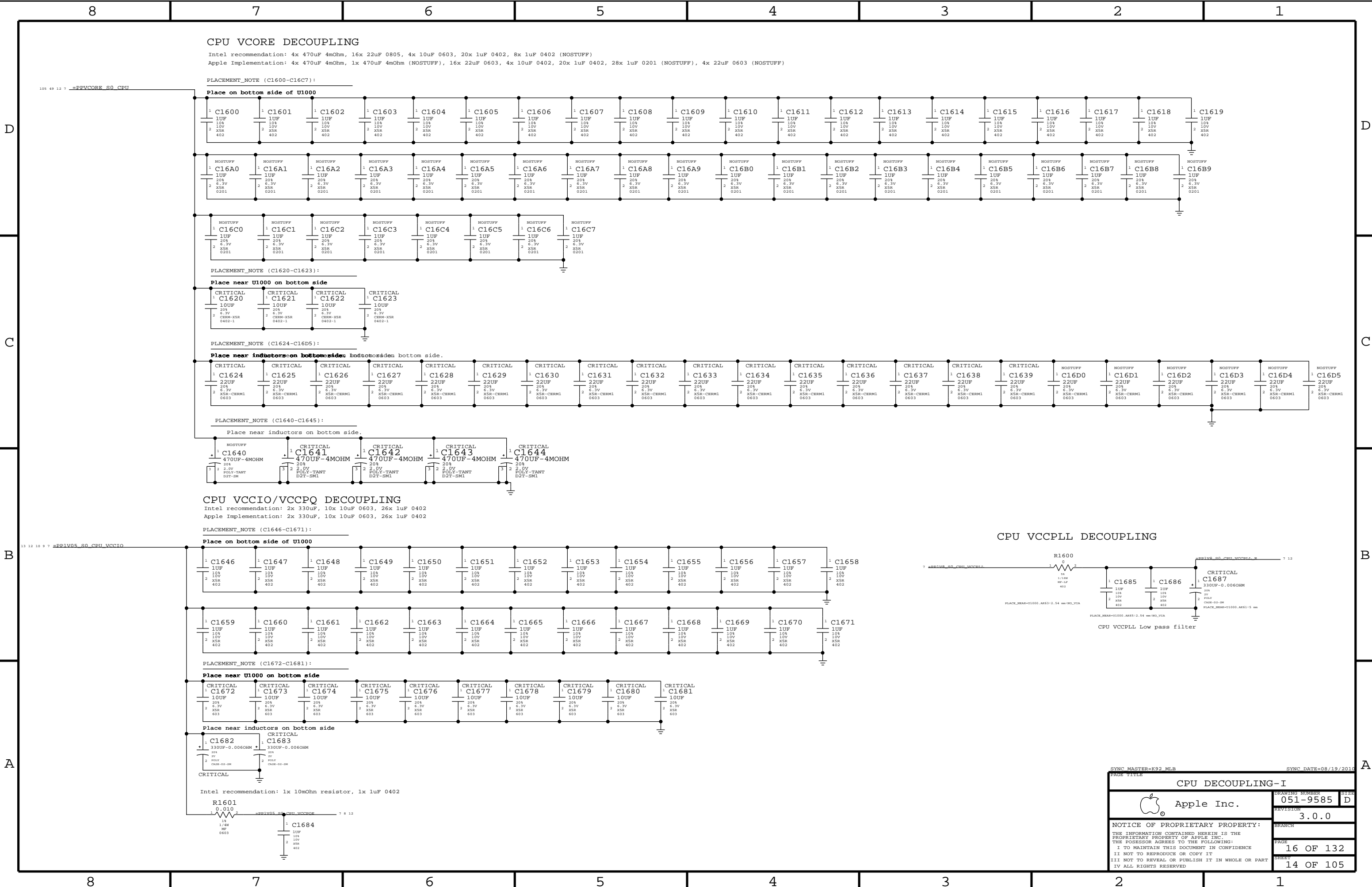




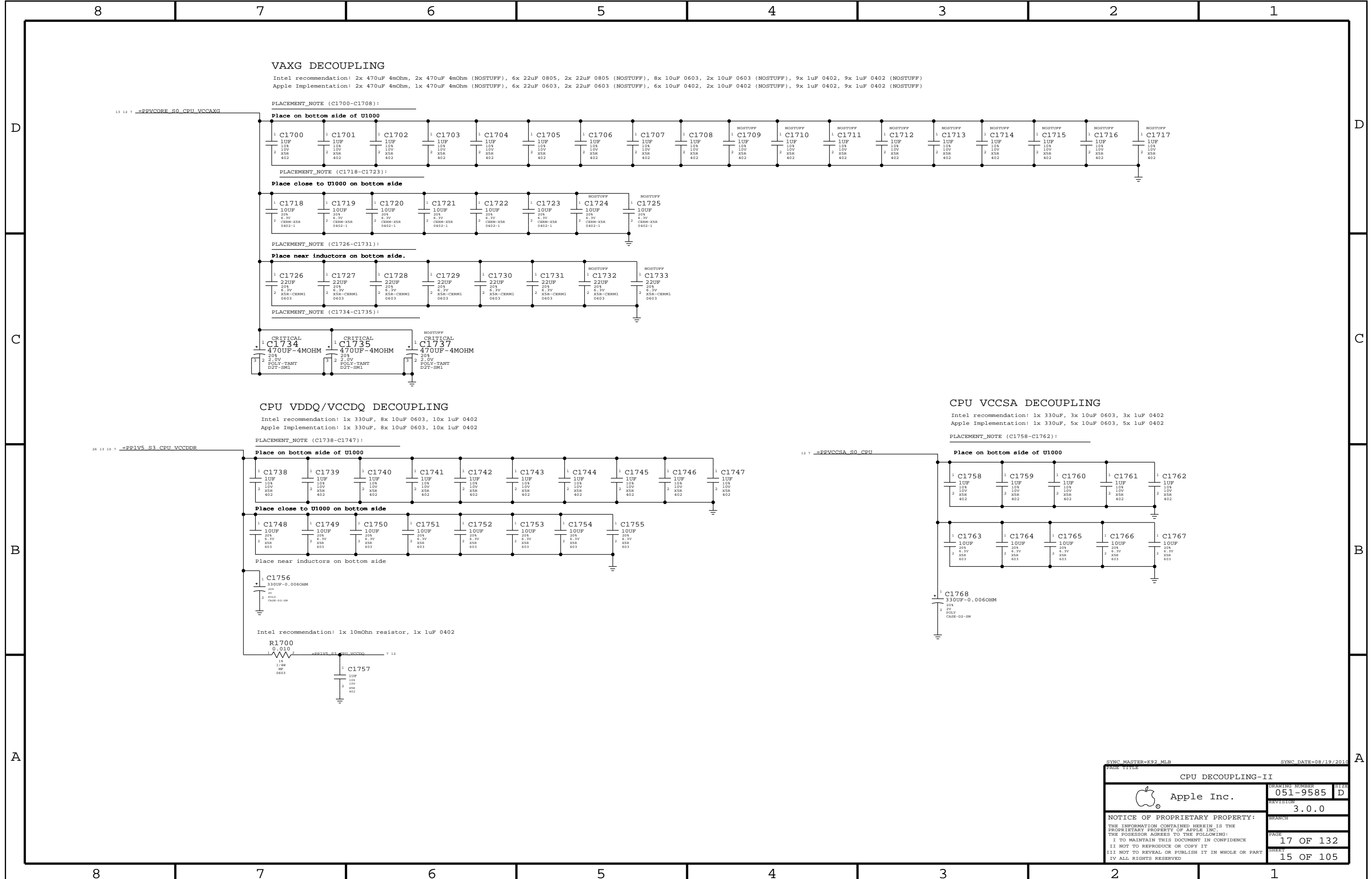


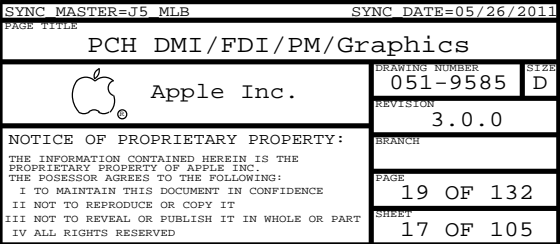
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

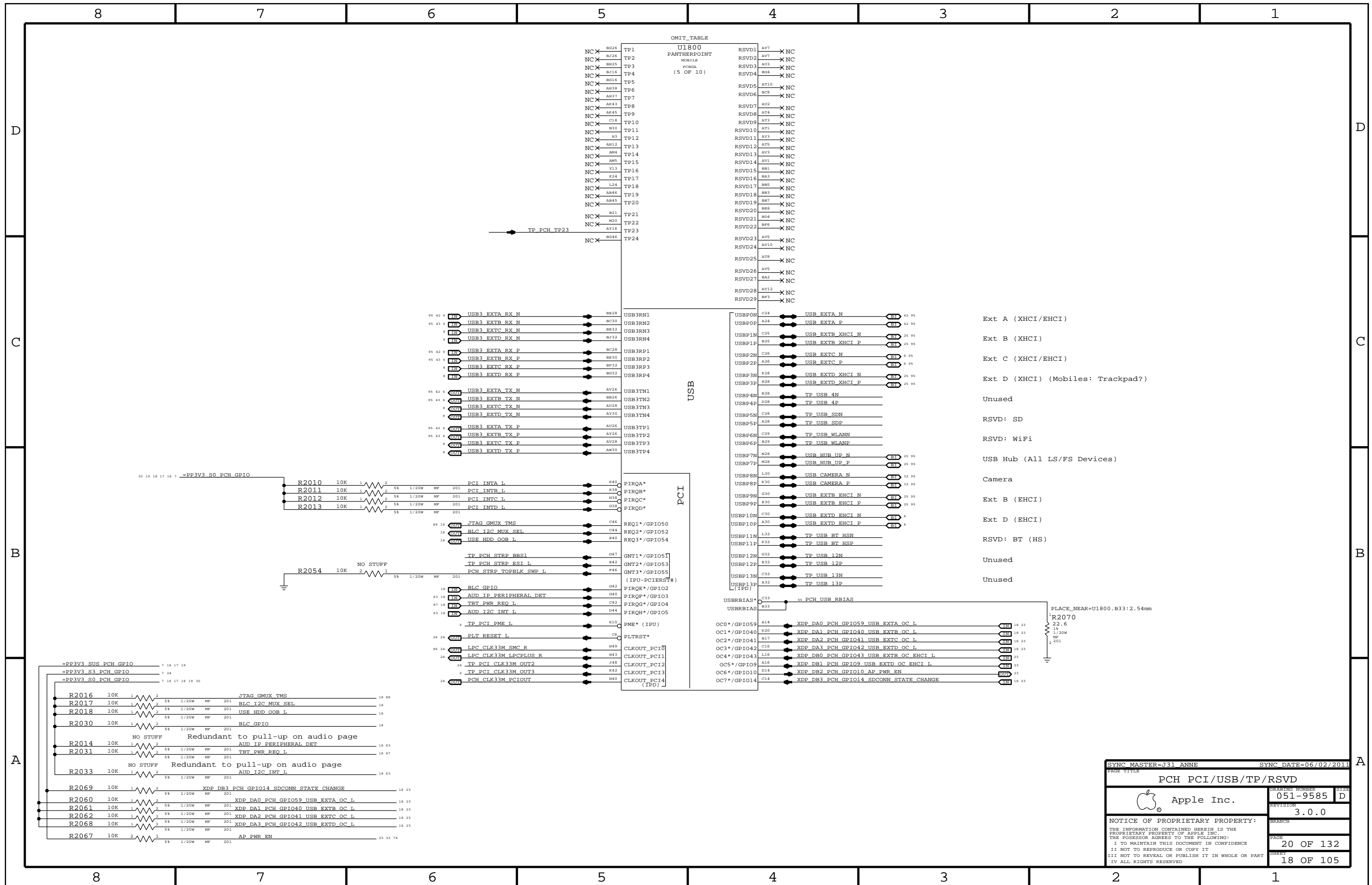


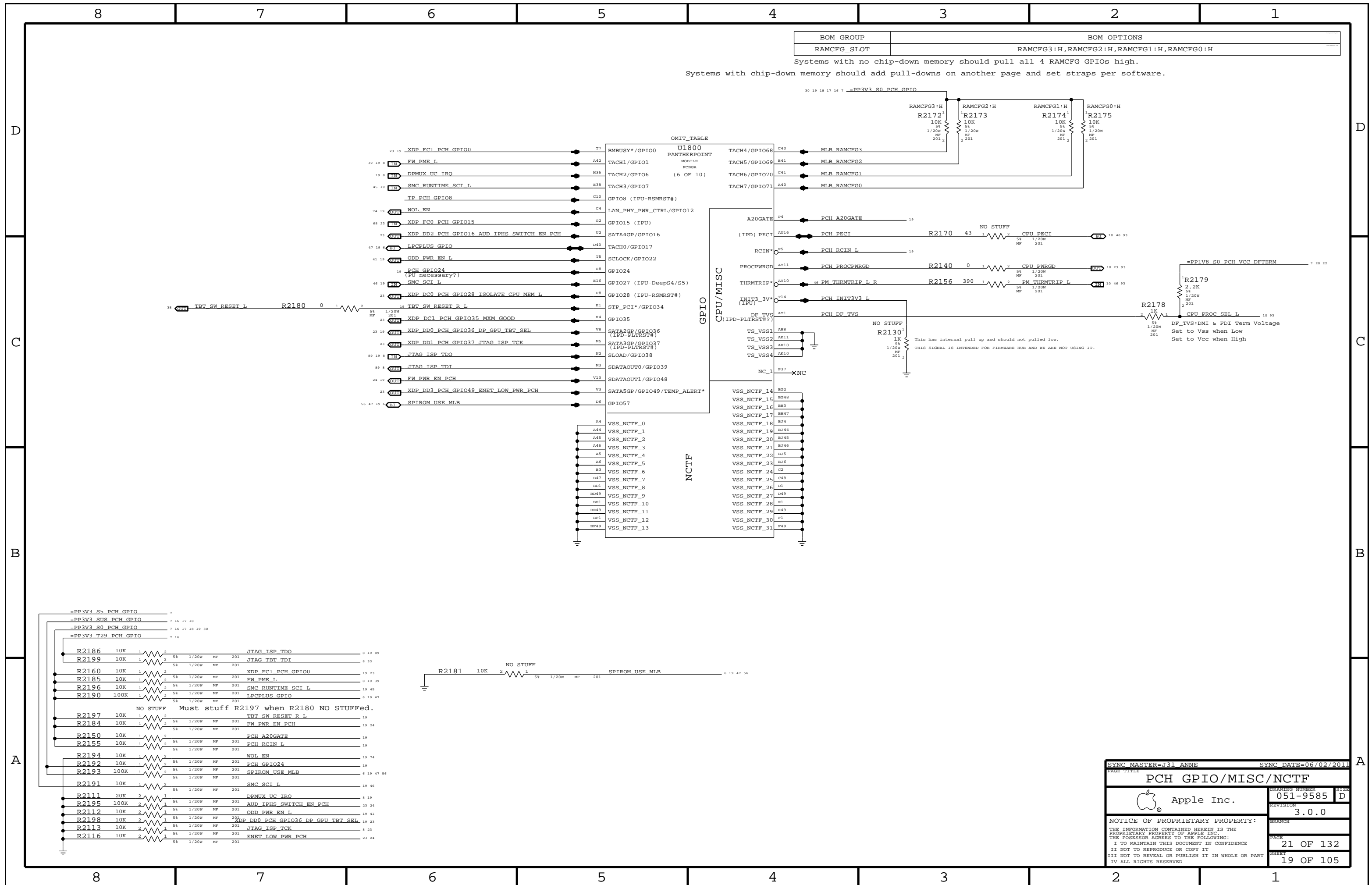


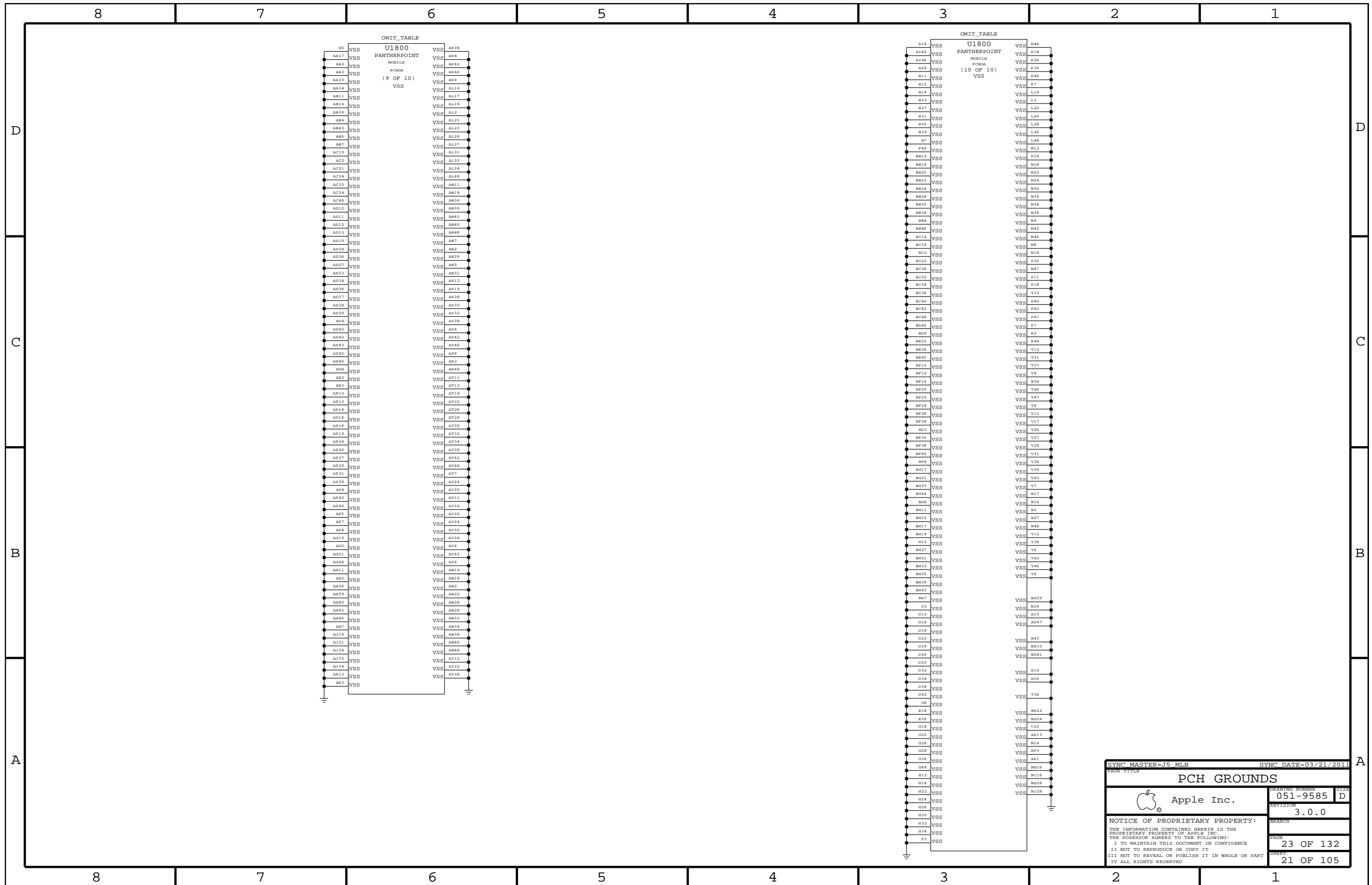
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CPU DECOUPLING-I		DRAWING NUMBER	051-9585
Apple Inc.		REVISION	3.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	16 OF 132
		SHEET	14 OF 105

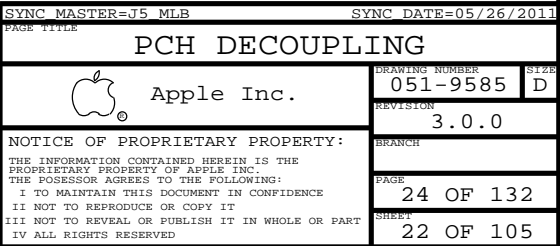


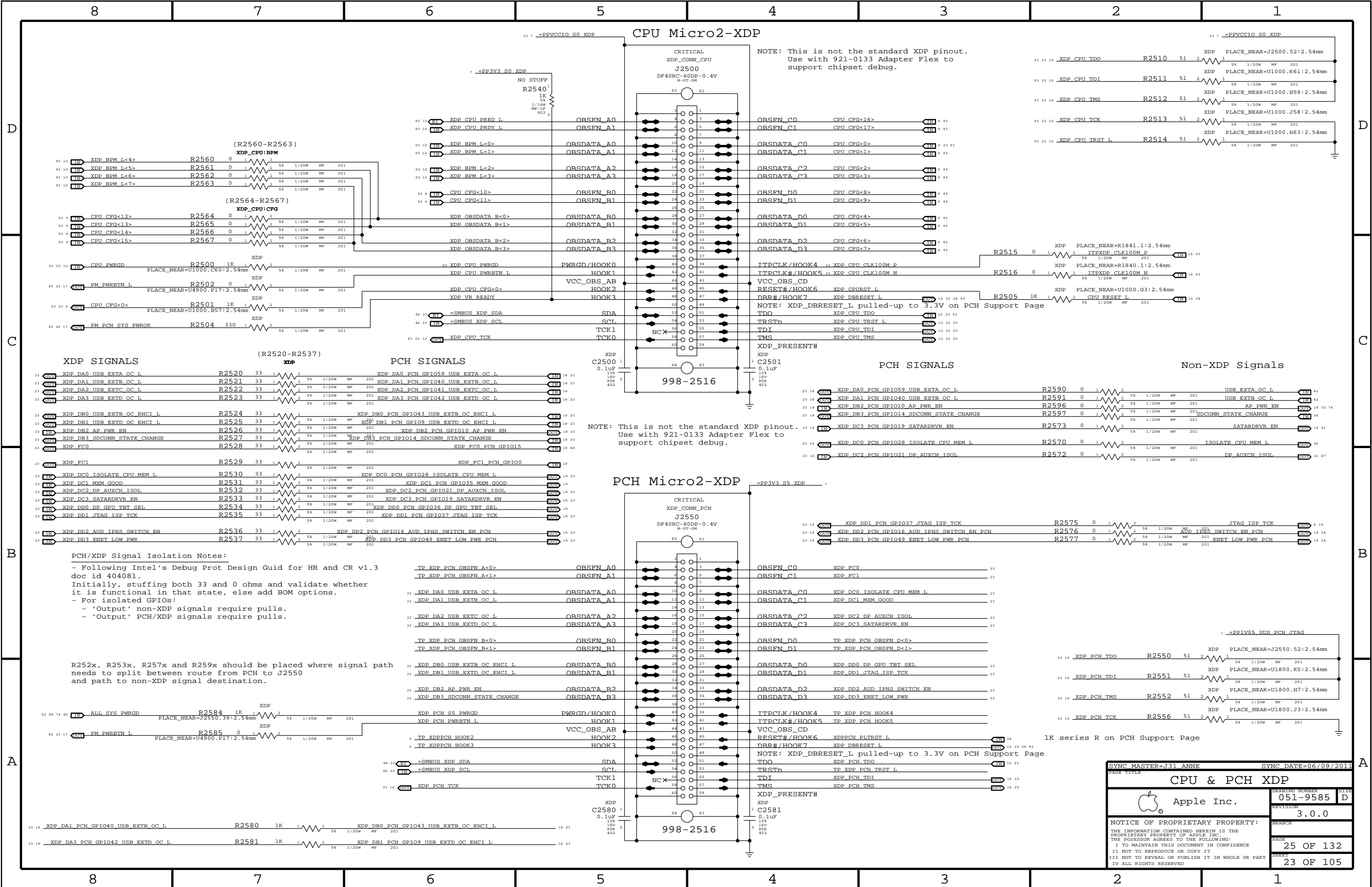










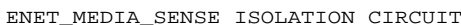
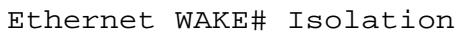


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B

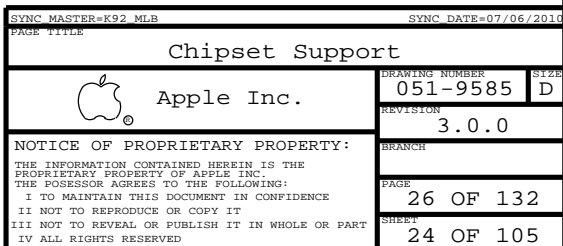
A



D



B



USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0, HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0, HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1, HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1, HUB_NONREM0_1

NON_REM 1 : NON_REM 0
 0 : 0
 1 : 1
 1 : 1

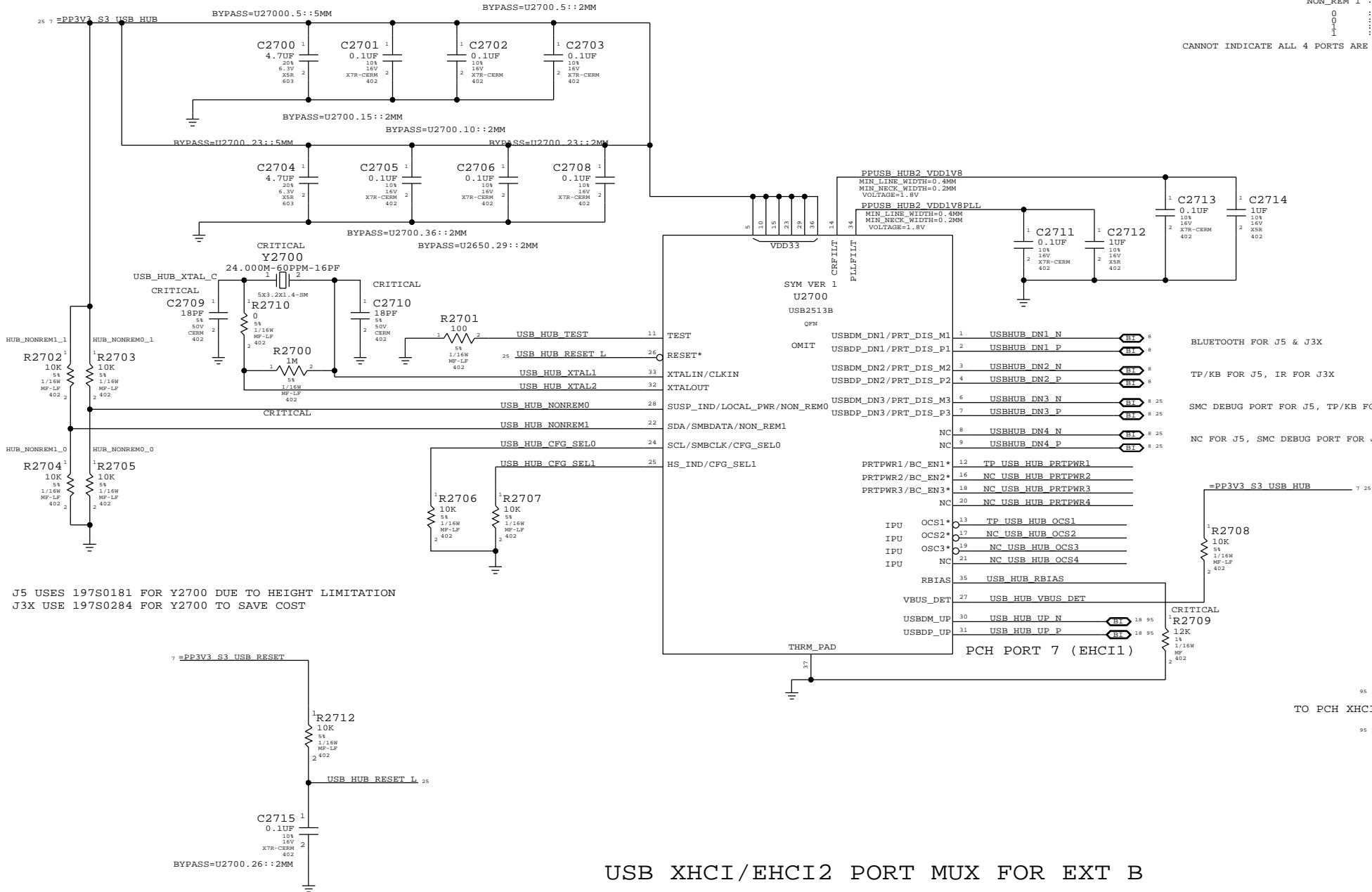
STRAP PIN CFG
 ALL PORTS ARE REMOVABLE
 PORT 1 IS NON REMOVABLE
 PORT 1&2 ARE NON REMOVABLE
 PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

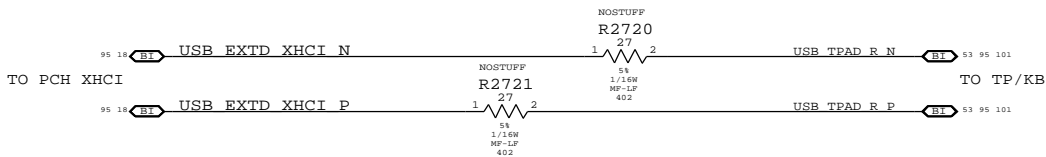
J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
 J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



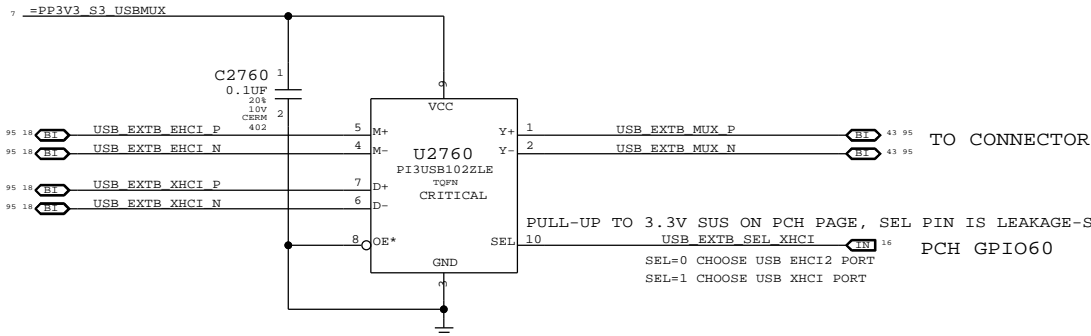
J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
 J3X USE 197S0284 FOR Y2700 TO SAVE COST

BLUETOOTH FOR J5 & J3X
 TP/KB FOR J5, IR FOR J3X
 SMC DEBUG PORT FOR J5, TP/KB FOR J3X
 NC FOR J5, SMC DEBUG PORT FOR J3X

TO CONNECT TP/KB TO PCH XHCI
 NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



PCH PORT 9 (EHCI2)

PCH PORT 1 (XHCI)

PAGE TITLE		PAGE NUMBER	
USB HUB & MUX		051-9585	
Apple Inc.		3.0.0	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

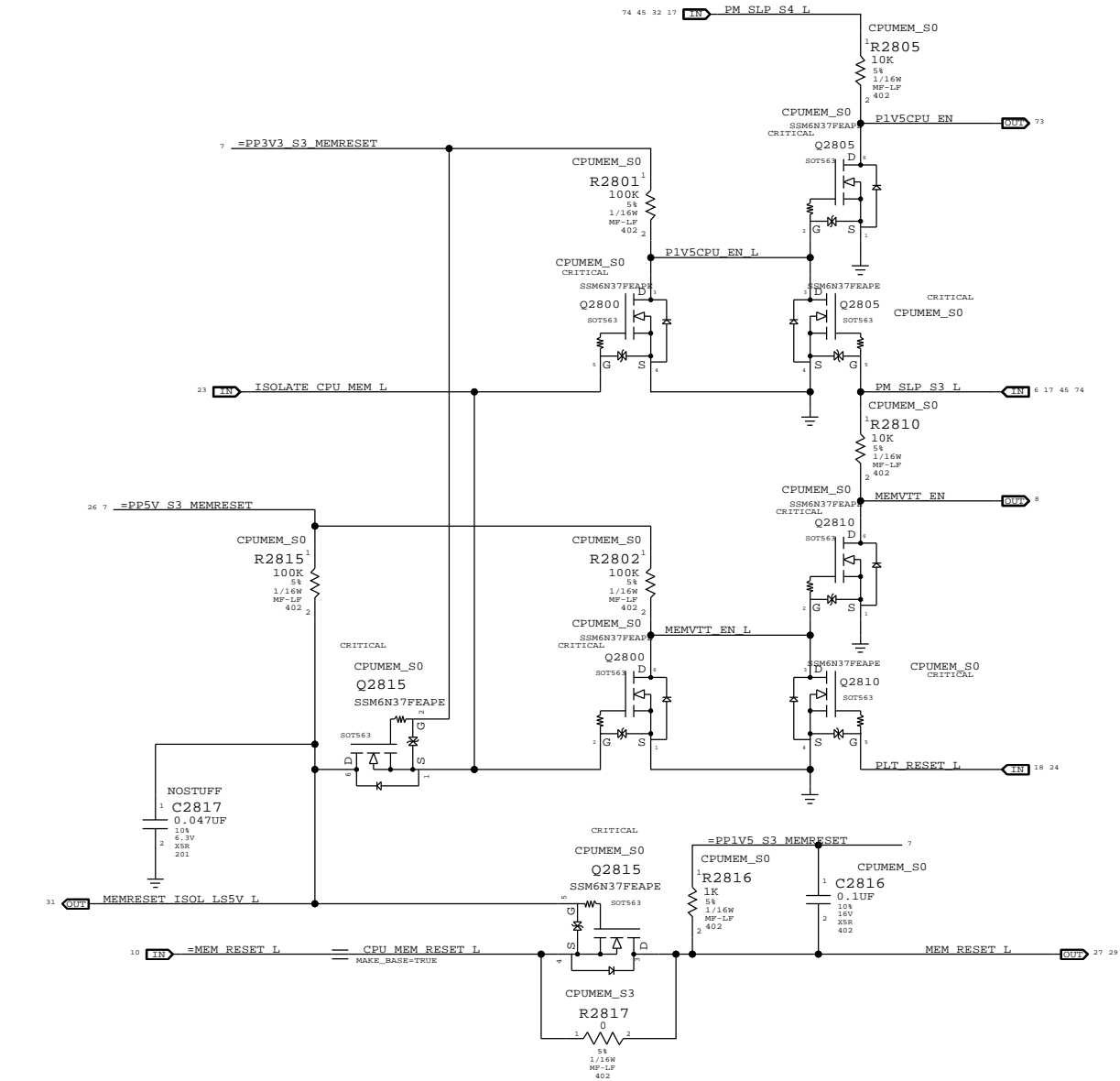
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

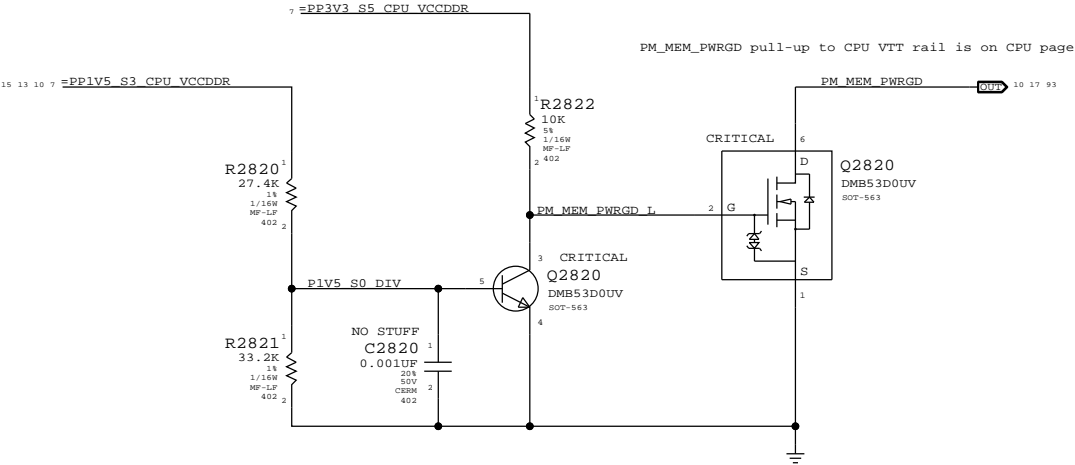


Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

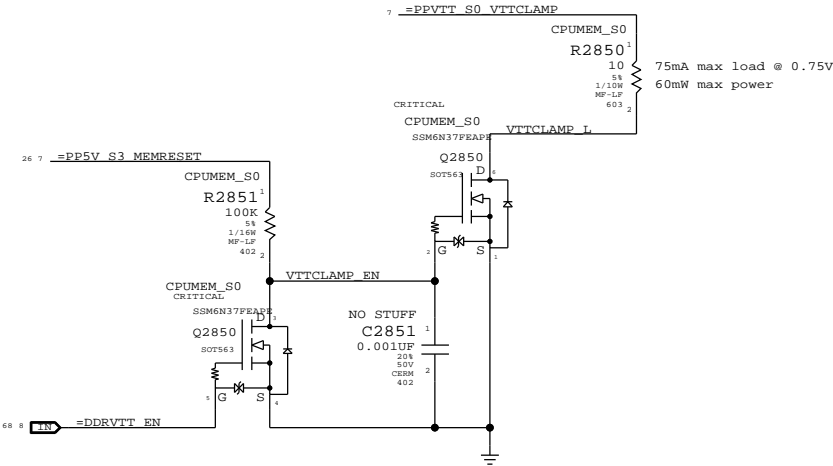
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.


1V5 S0 "PGOOD" for CPU

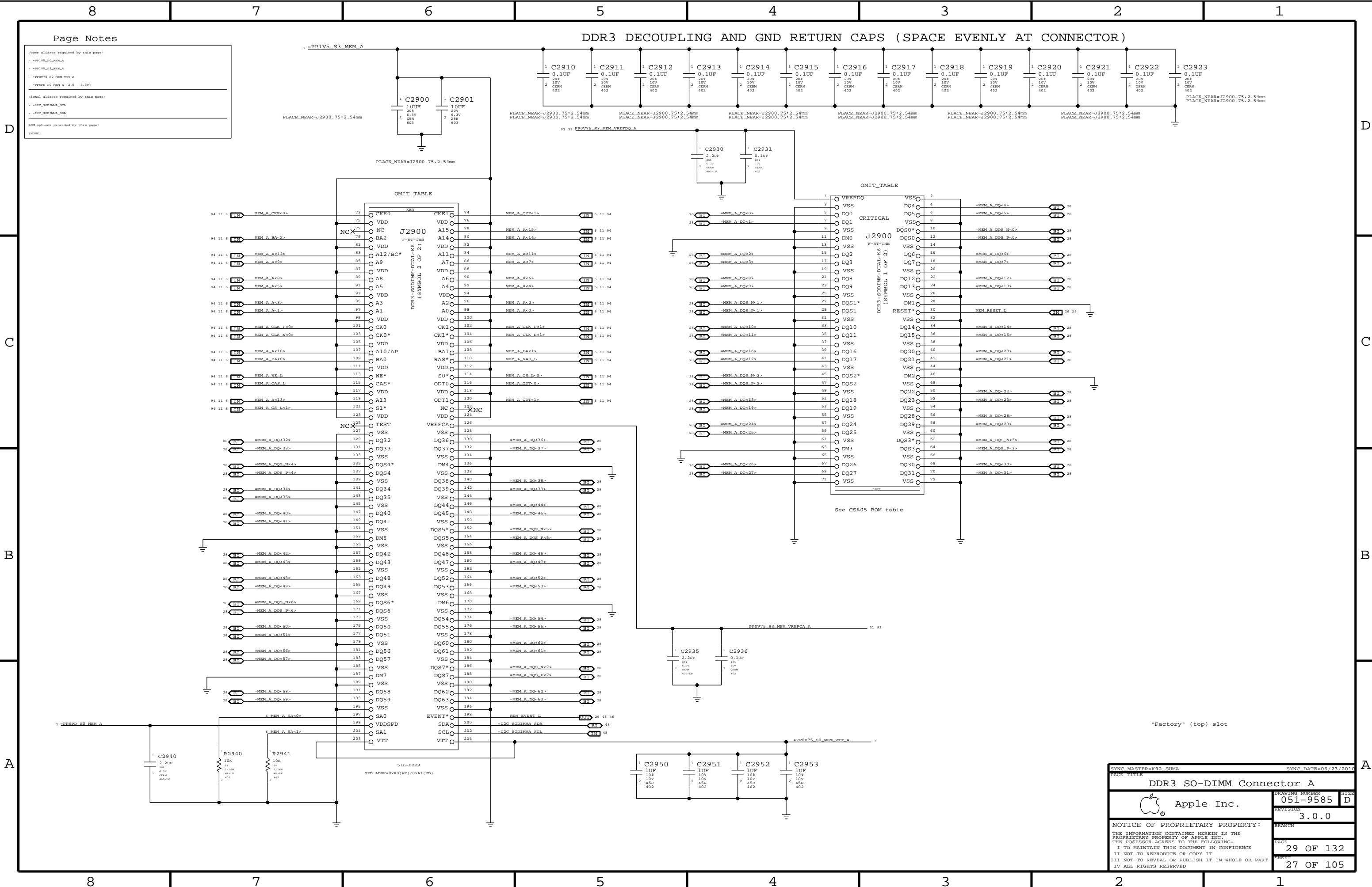


MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC MASTER=K18 MLB		SYNC DATE=04/27/2010	
PAGE TITLE			
CPU Memory S3 Support			
 Apple Inc.		DRAWING NUMBER	051-9585
		SIZE	D
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:


- PPIV5_S3_MEM_A
- PPIV5_S3_MEM_A
- PPIV5_S3_MEM_VTT_A
- PPIV5_S3_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_SODIMMA_SCL
- I2C_SODIMMA_SDA

DOM options provided by this page:

(None)

SYNC MASTER=K92 SUMA		SYNC DATE=06/23/2010	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-9585	D
		REVISION	
		3.0.0	
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27 OF 105			
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8		7		6		5		4		3		2		1														
D	CPU CHANNEL A DQS 0 -> DIMM A DQS 0														CPU CHANNEL B DQS 0 -> DIMM B DQS 0													
	94 11 6	MEM_A_DQS_N<0>	=====	=MEM_A_DQS_N<0>	27	94 11 6	MEM_B_DQS_N<0>	=====	=MEM_B_DQS_N<0>	29																		
	94 11 6	MEM_A_DQS_P<0>	=====	=MEM_A_DQS_P<0>	27	94 11 6	MEM_B_DQS_P<0>	=====	=MEM_B_DQS_P<0>	29																		
	94 11 6	MEM_A_DQ<7>	=====	=MEM_A_DQ<3>	27	94 11 6	MEM_B_DQ<7>	=====	=MEM_B_DQ<6>	29																		
	94 11 6	MEM_A_DQ<6>	=====	=MEM_A_DQ<6>	27	94 11 6	MEM_B_DQ<6>	=====	=MEM_B_DQ<3>	29																		
	94 11 6	MEM_A_DQ<5>	=====	=MEM_A_DQ<5>	27	94 11 6	MEM_B_DQ<5>	=====	=MEM_B_DQ<5>	29																		
	94 11 6	MEM_A_DQ<4>	=====	=MEM_A_DQ<4>	27	94 11 6	MEM_B_DQ<4>	=====	=MEM_B_DQ<4>	29																		
	94 11 6	MEM_A_DQ<3>	=====	=MEM_A_DQ<7>	27	94 11 6	MEM_B_DQ<3>	=====	=MEM_B_DQ<1>	29																		
	94 11 6	MEM_A_DQ<2>	=====	=MEM_A_DQ<0>	27	94 11 6	MEM_B_DQ<2>	=====	=MEM_B_DQ<7>	29																		
C	CPU CHANNEL A DQS 1 -> DIMM A DQS 1														CPU CHANNEL B DQS 1 -> DIMM B DQS 1													
	94 11 6	MEM_A_DQS_N<1>	=====	=MEM_A_DQS_N<1>	27	94 11 6	MEM_B_DQS_N<1>	=====	=MEM_B_DQS_N<1>	29																		
	94 11 6	MEM_A_DQS_P<1>	=====	=MEM_A_DQS_P<1>	27	94 11 6	MEM_B_DQS_P<1>	=====	=MEM_B_DQS_P<1>	29																		
	94 11 6	MEM_A_DQ<15>	=====	=MEM_A_DQ<15>	27	94 11 6	MEM_B_DQ<15>	=====	=MEM_B_DQ<15>	29																		
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	94 11 6	MEM_A_DQ<12>	=====	=MEM_A_DQ<13>	27	94 11 6	MEM_B_DQ<12>	=====	=MEM_B_DQ<12>	29																		
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	94 11 6	MEM_A_DQ<10>	=====	=MEM_A_DQ<11>	27	94 11 6	MEM_B_DQ<10>	=====	=MEM_B_DQ<10>	29																		
B	CPU CHANNEL A DQS 2 -> DIMM A DQS 2														CPU CHANNEL B DQS 2 -> DIMM B DQS 2													
	94 11 6	MEM_A_DQS_N<2>	=====	=MEM_A_DQS_N<2>	27	94 11 6	MEM_B_DQS_N<2>	=====	=MEM_B_DQS_N<2>	29																		
	94 11 6	MEM_A_DQS_P<2>	=====	=MEM_A_DQS_P<2>	27	94 11 6	MEM_B_DQS_P<2>	=====	=MEM_B_DQS_P<2>	29																		
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	94 11 6	MEM_A_DQ<19>	=====	=MEM_A_DQ<19>	27	94 11 6	MEM_B_DQ<19>	=====	=MEM_B_DQ<19>	29																		
	94 11 6	MEM_A_DQ<18>	=====	=MEM_A_DQ<18>	27	94 11 6	MEM_B_DQ<18>	=====	=MEM_B_DQ<18>	29																		
A	CPU CHANNEL A DQS 3 -> DIMM A DQS 3														CPU CHANNEL B DQS 3 -> DIMM B DQS 3													
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	94 11 6	MEM_A_DQS_P<3>	=====	=MEM_A_DQS_P<3>	27	94 11 6	MEM_B_DQS_P<3>	=====	=MEM_B_DQS_P<3>	29																		
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DDR3 MASTER-K92-000A

DDR3 Byte/Bit Swaps

Apple Inc.

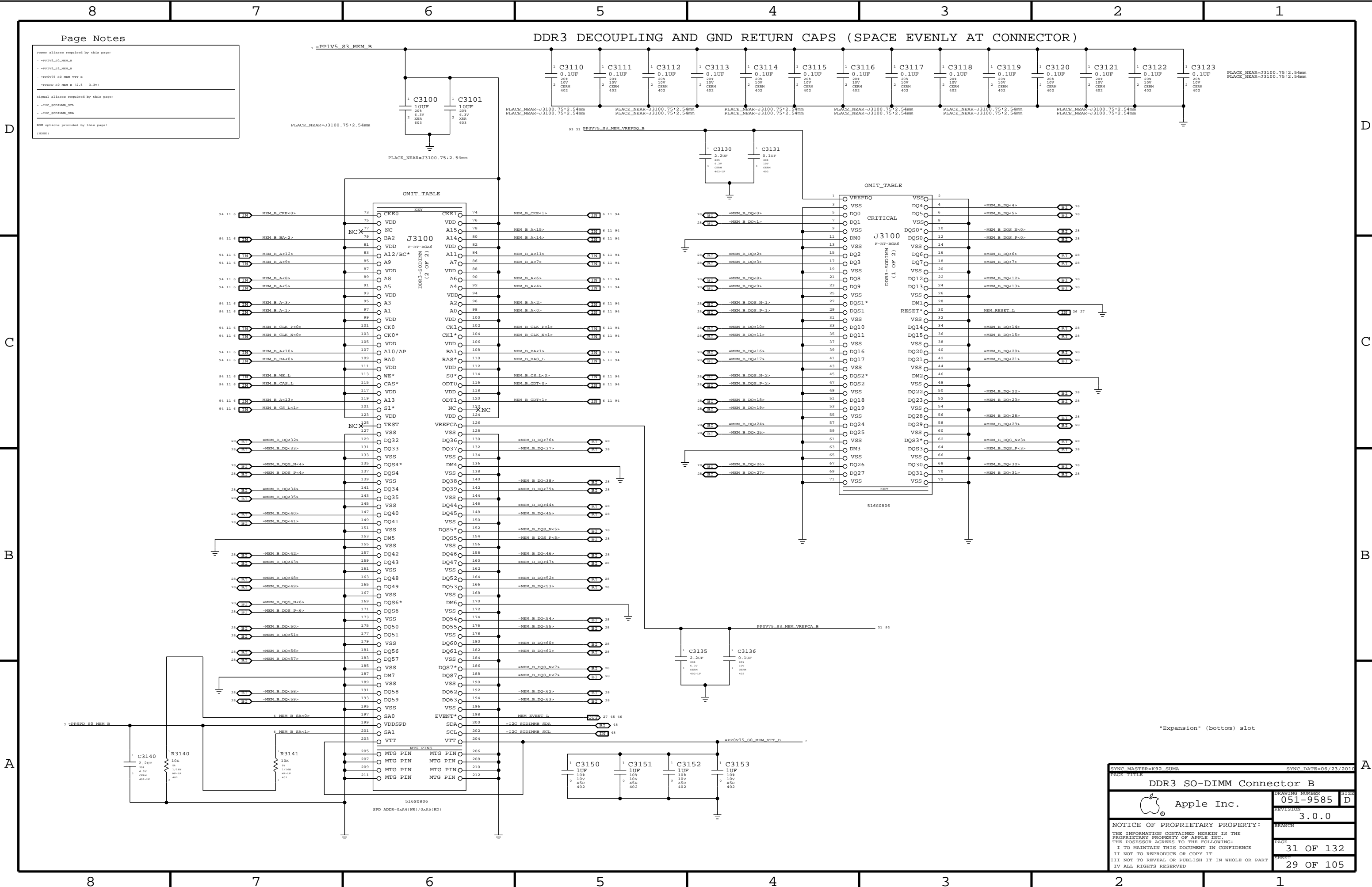
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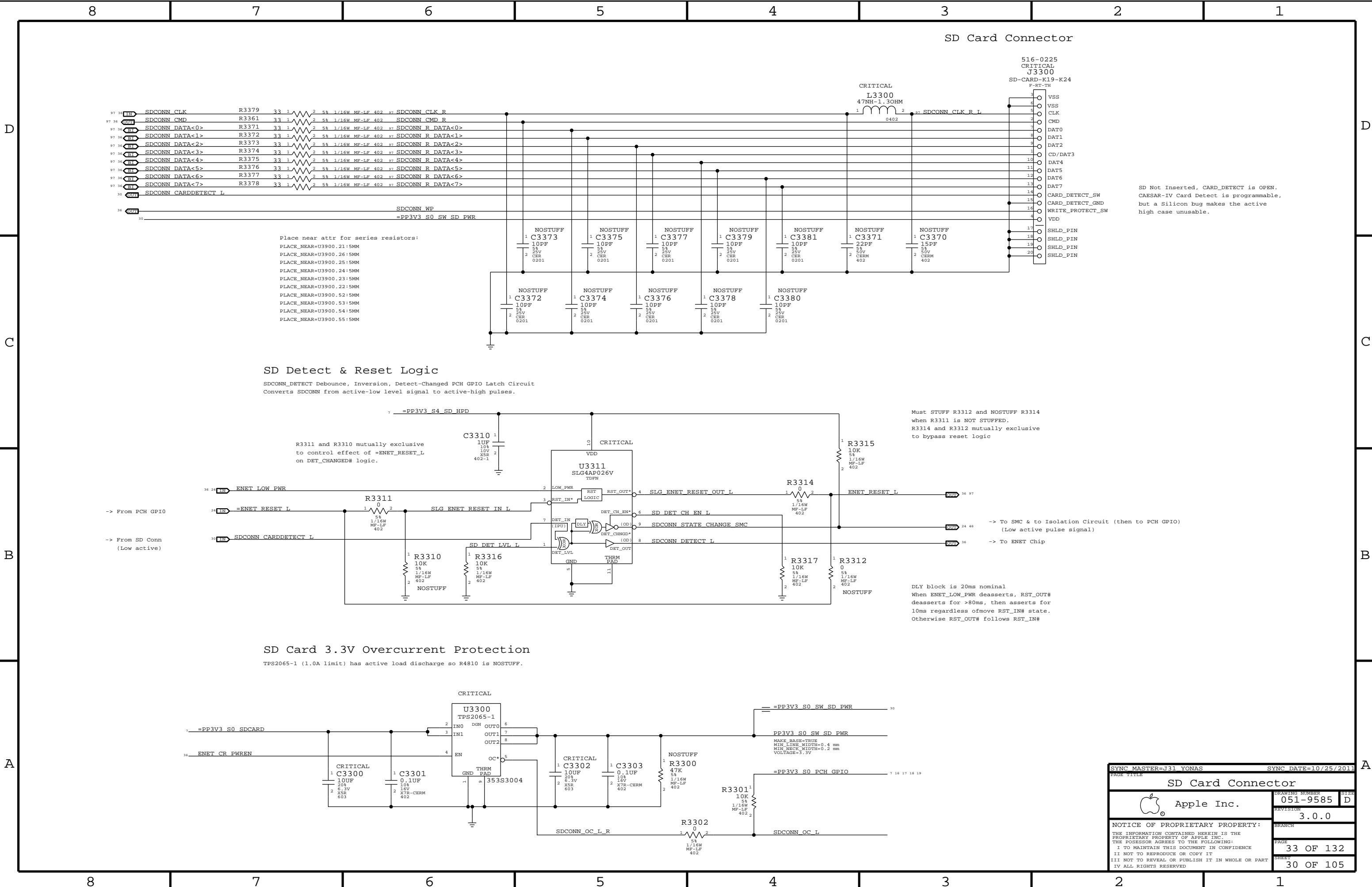
Page Notes

Power aliases required by this page:
- ~PP1V5_S3_MEM_B
- ~PP1V5_S3_MEM_B
- ~PP0V75_S3_MEM_VTT_B
- ~PPSPD_S0_MEM_B (2.5 - 3.3V)
Signal aliases required by this page:
- ~I2C_S0D1MMB_SCL
- ~I2C_S0D1MMB_SDA
BOM options provided by this page:
(None)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

"Expansion" (bottom) slot

SYNC MASTER=K92 SUMA		SYNC DATE=06/23/2010	
PAGE TITLE			
DDR3 SO-DIMM Connector B		DRAWING NUMBER	SHEET
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		3.0.0	
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SD Card Connector		051-9585		D	
REVISION		3.0.0		BRANCH	
PAGE		33 OF 132		SHEET	
30 OF 105					

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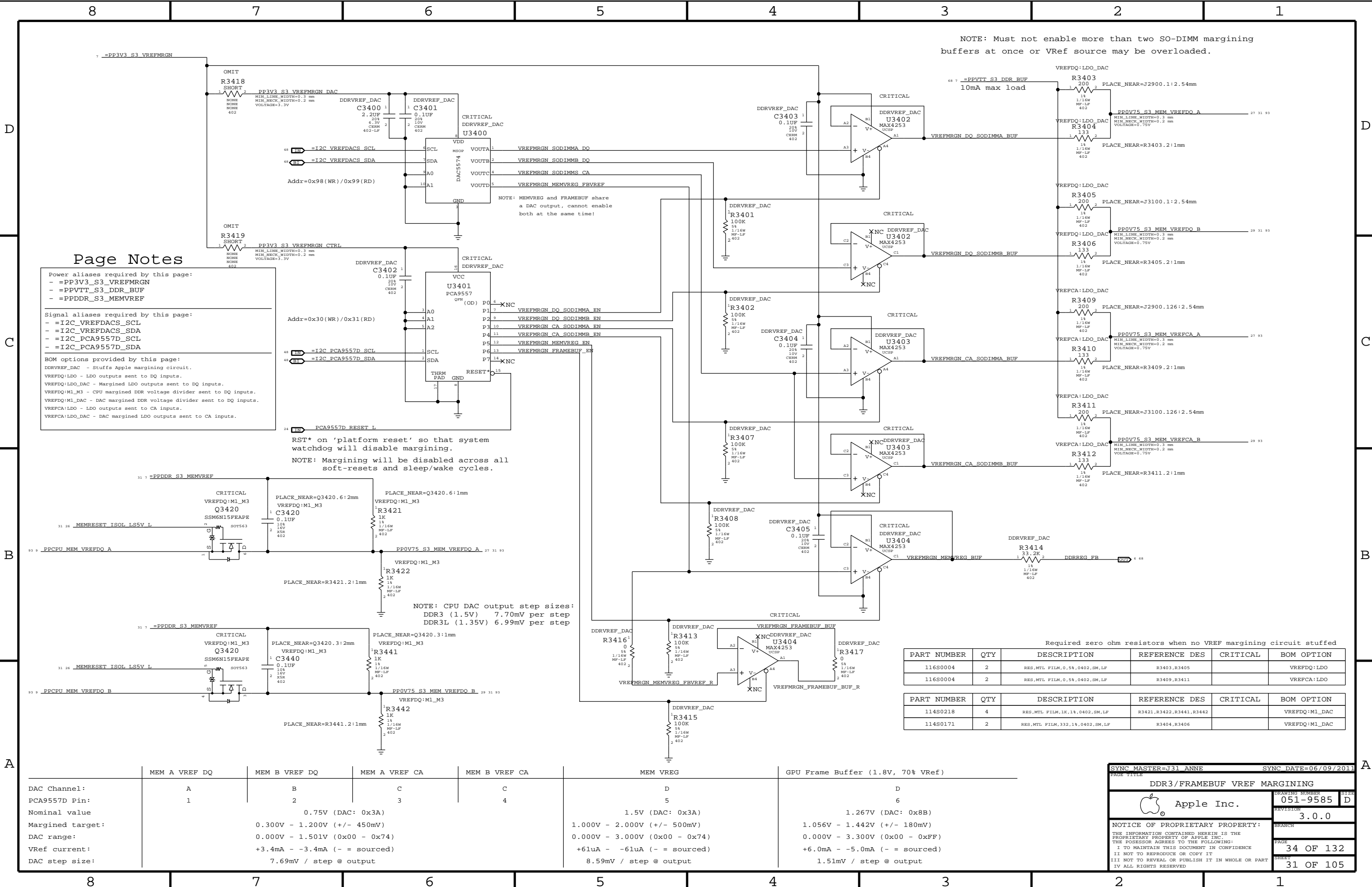
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.000V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J31 ANNE

SYNC DATE=06/09/2011

DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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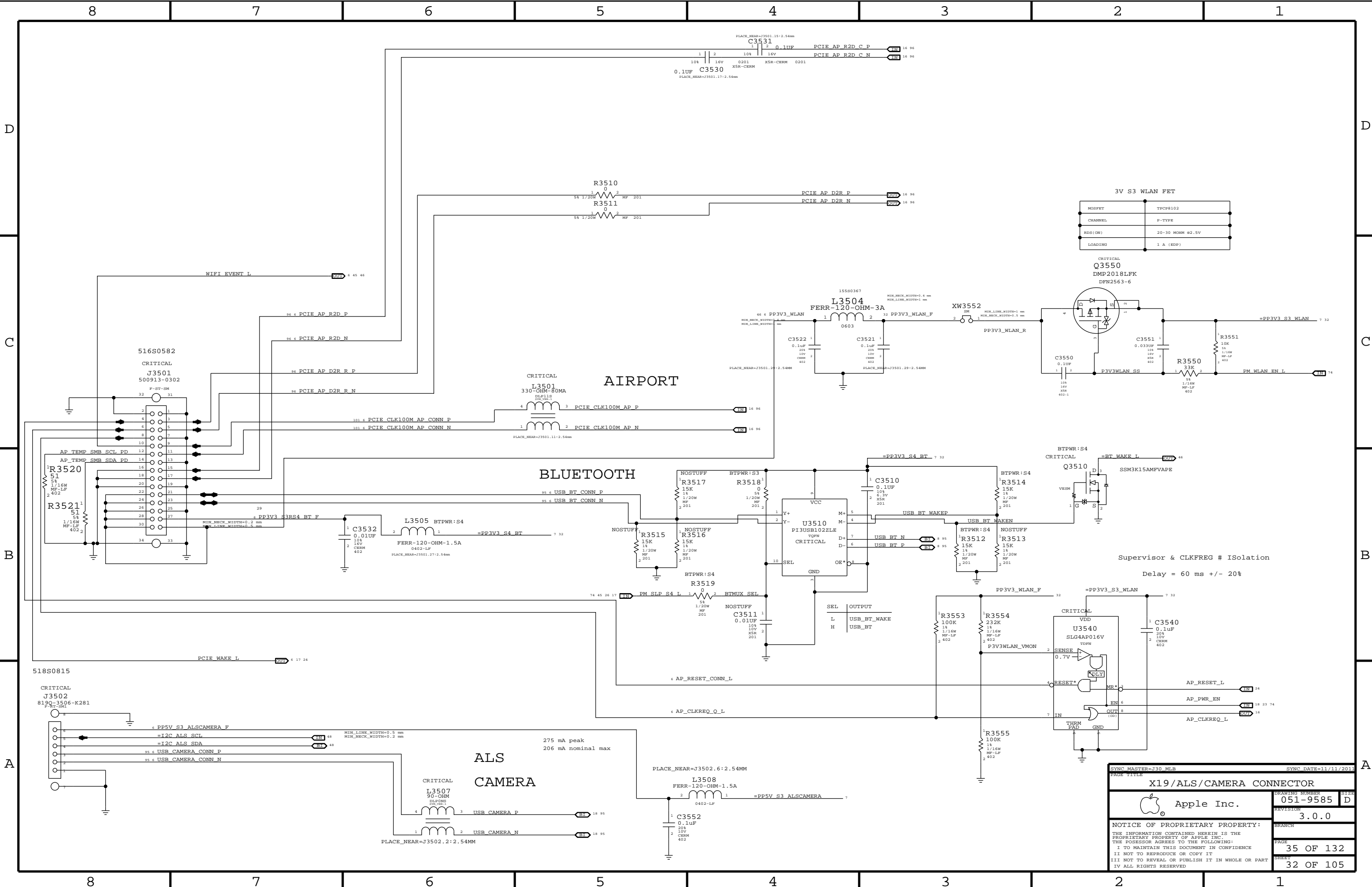
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
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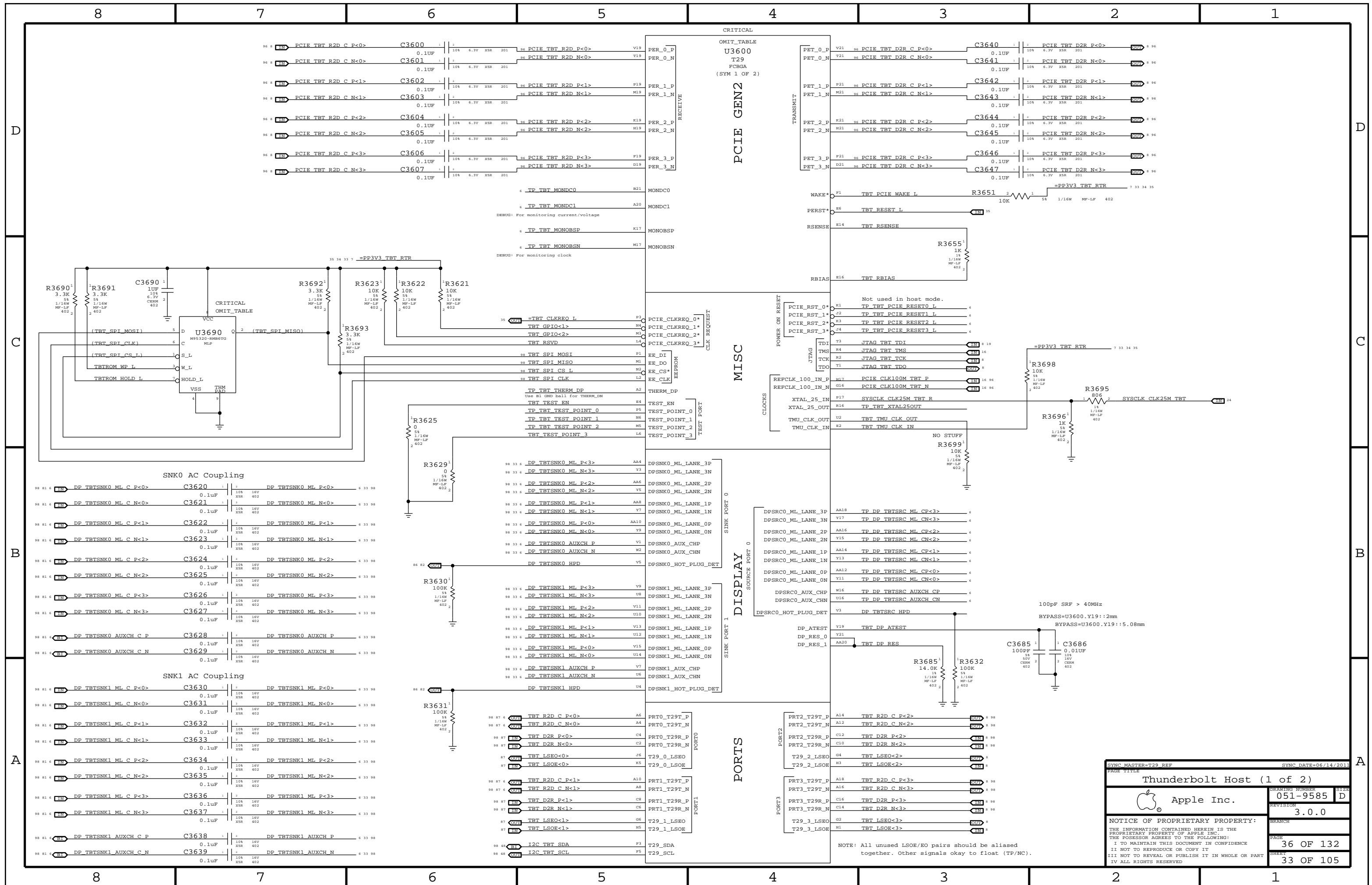
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SHEET

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SYNC MASTER=J30 MLB		SYNC DATE=11/11/2011	
PAGE TITLE			
X19/ALS/CAMERA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-9585	D
		REVISION	
		3.0.0	
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6

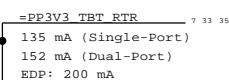
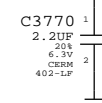
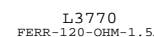
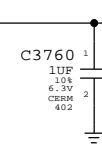
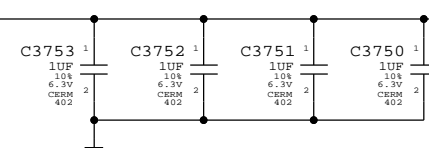
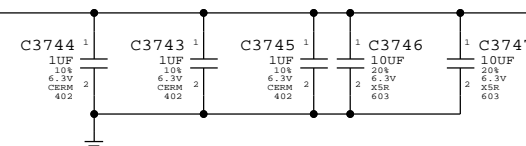
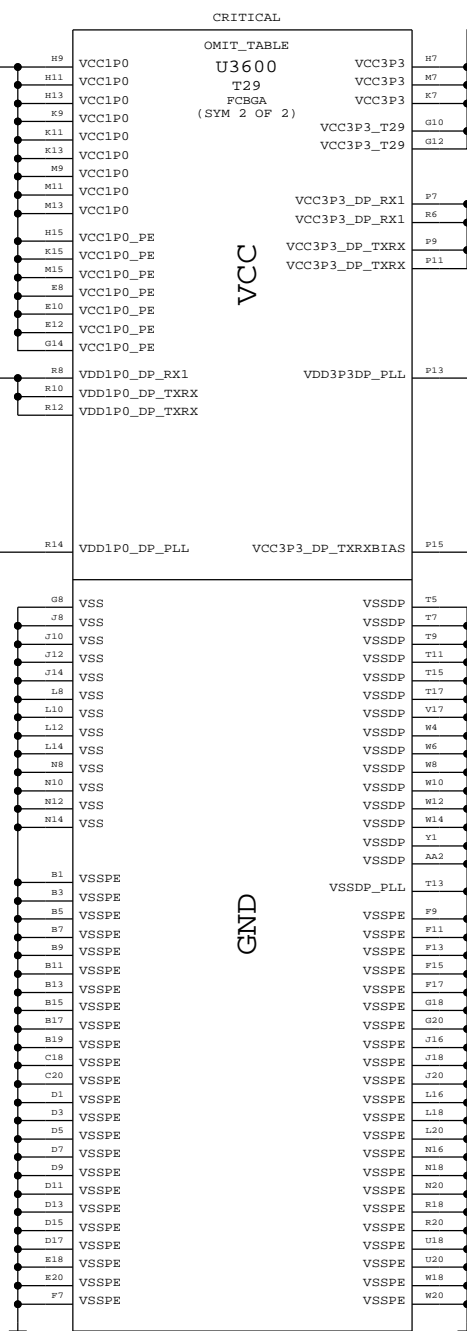
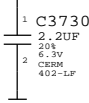
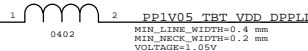
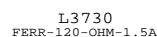
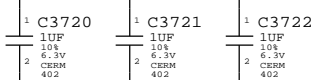
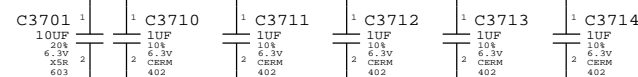
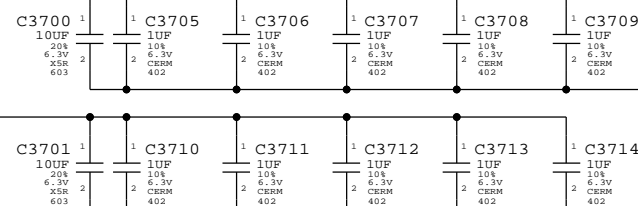
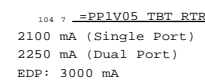
(5)

4

(a)

2

—



```

Power aliases required by this page:
- =PPVIN_SW_TBTBST      (8-13V Boost Input)
- =PP15V_TBT_REG        (15V Boost Output)
- =PP3V3_S0_P3V3TBTFTF (3.3V FET Input)
- =PP3V3_TBT_FET        (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_S0_P1V05TBTFTF (1.05V FET Input)
- =PP1V05_TBT_FET       (1.05V FET Output)

```

```

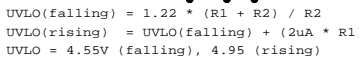
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

```

```

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

```



7 =PP3V3 S0 TBTWRCRL

Platform (PCIe) Reset

24 =TBT RESET L

Open-Drain GPIO

19 =TBT SW RESET L

24 =TBT PWR EN

16 =TBT CLKREQ L

Pull-ups provided by SB page.

C3800 0.1UF 10V 25V X5R 402

R3803 10K 5% 1/16W 0P-LP 402

R3807 10K 5% 1/16W 0P-LP 402

U3800 SLG4AP016V TDFN

VDD

SENSE 0.7V

MR*

EN

OUT (OD)

GND

THERM PAD

CRITICAL

PP3V3 TBT_RTR

PP1V05 TBT

TBT RESET L

DLY = 60 ms +/- 20%

=TBT CLKREQ L

TBT CLKREQ ISOL L

MAKE_BASE=TRUE

U3810
TPS22924
CSP

Part TPS22924C


Type	Load Switch
R(on)	18.3 mOhm Typ
@ 2.5V	24 mOhm Max

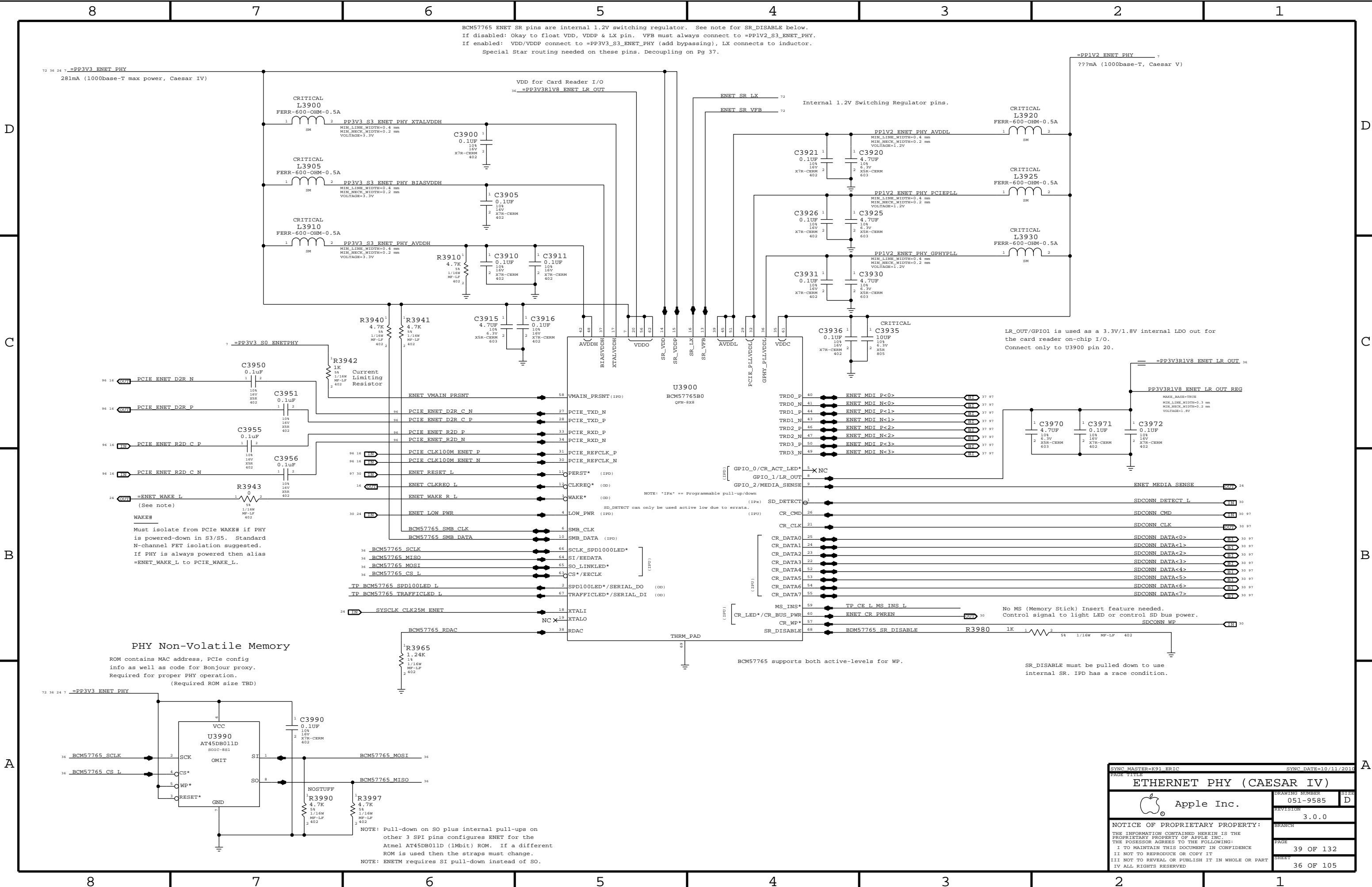
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

[illegible]

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max

[illegible]

SYNCH MASTER=T29 REF		SYNCH DATE=06/22/2011	
PAGE TITLE			
Thunderbolt Power Support			
 Apple Inc.	DRAWING NUMBER	051-9585	SIZE D
	REVISION	3.0.0	
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

SYNC MASTER=K91 ERIC		SYNC DATE=10/11/2010	
PAGE TITLE		DRAWING NUMBER	
ETHERNET PHY (CAESAR IV)		051-9585	
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

97 36 ENET MDI P<0>

97 36 ENET MDI N<0>

97 36 ENET MDI N<1>

97 36 ENET MDI P<1>

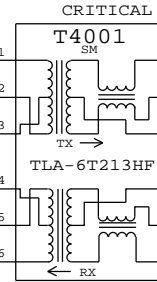
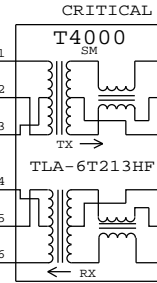
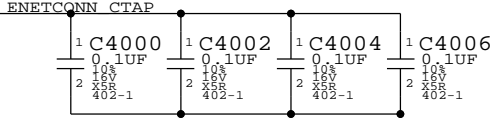
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97 36 ENET MDI P<2>

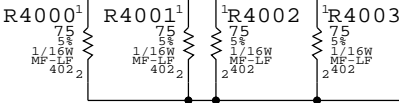
97 36 ENET MDI N<3>

97 36 ENET MDI P<3>

Place one of 0.1uF cap close to each centertap pin of transformer



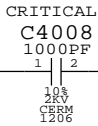
Transformers should be mirrored on opposite sides of the board



ENET BOB SMITH CAP

MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.25 mm



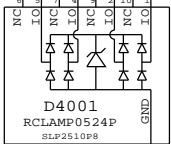
CRITICAL

J4000

RJ45-M97-3

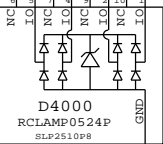
F-RT-TH

514-0636



CRITICAL

NOSTUFF



CRITICAL

NOSTUFF

PLACE_NEAR=T4001.1:5mm

PLACE_NEAR=T4000.5:5mm

Ethernet Connector



Apple Inc.

DRAWING NUMBER

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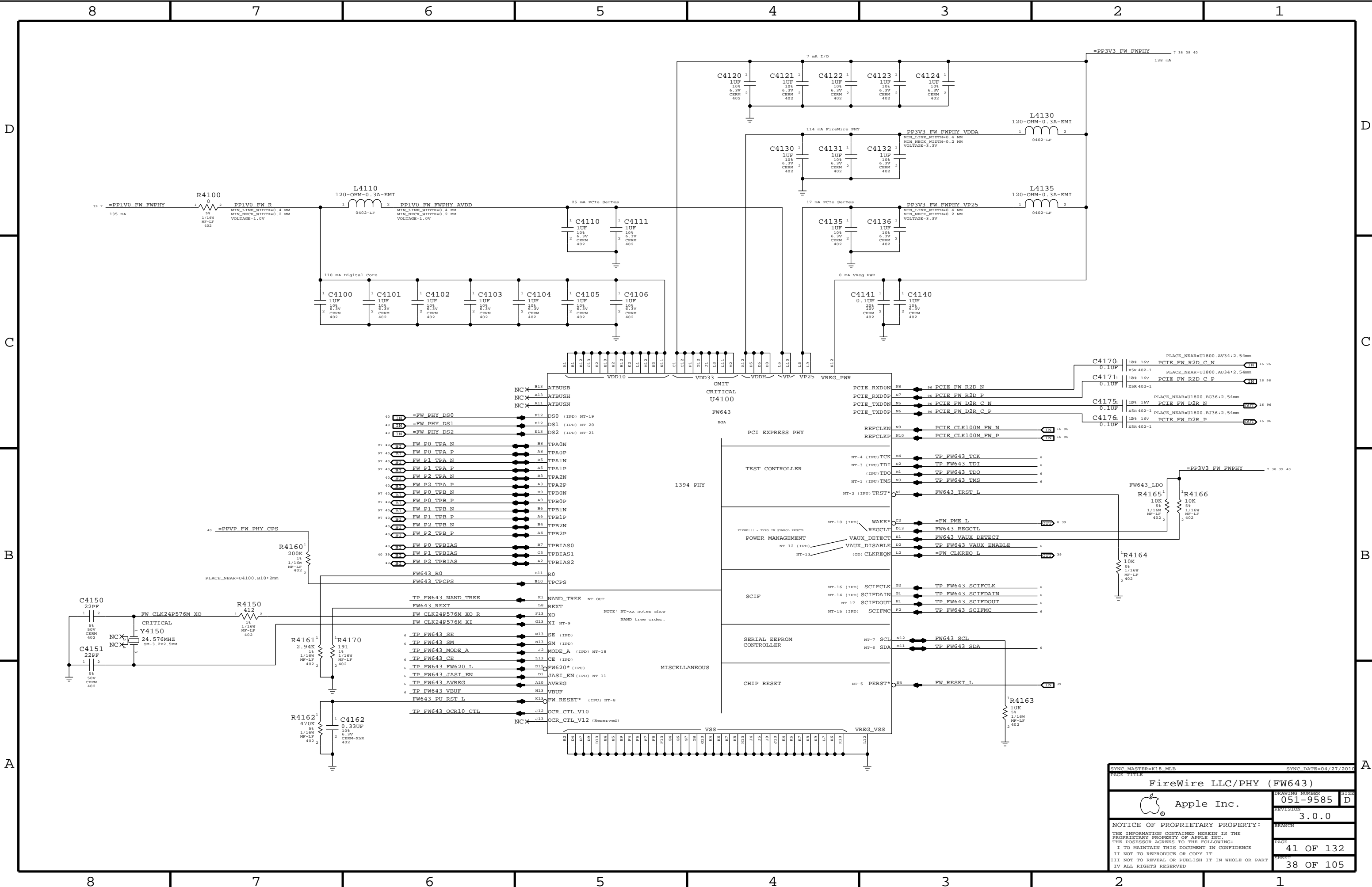
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Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PPL1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PPL1V05_FW_P1V0FWFET (1.0V FET Input)
- =PPL1V0_FW_FET_R (1.0V FET Output)
- =PPL1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:

(NONE)

[illegible][illegible][illegible]

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

Pull-up provided on another page.

3 CRITICAL

Max Output: 2A

U4201
TPS22924
CSP

PP3V3 FW P3V3VFWET

A2
B2
VIN

C4201
1 1uF
2 104
6.3V
CERM
402

ON
GND

A1
B1


PP3V3 FW FET

Max Current = 1.7A (85°C)

U4201

Part
Type
R(on)

[illegible]

SYNCH MASTER#K91 MLB		SYNCH DATE=06/17/2011	
PAGE TITLE			
FireWire Port & PHY Power			
	Apple Inc.		DRAWING NUMBER 051-9585
			SIZE D
		REVISION 3.0.0	
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		SHEET 39 OF 105	

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

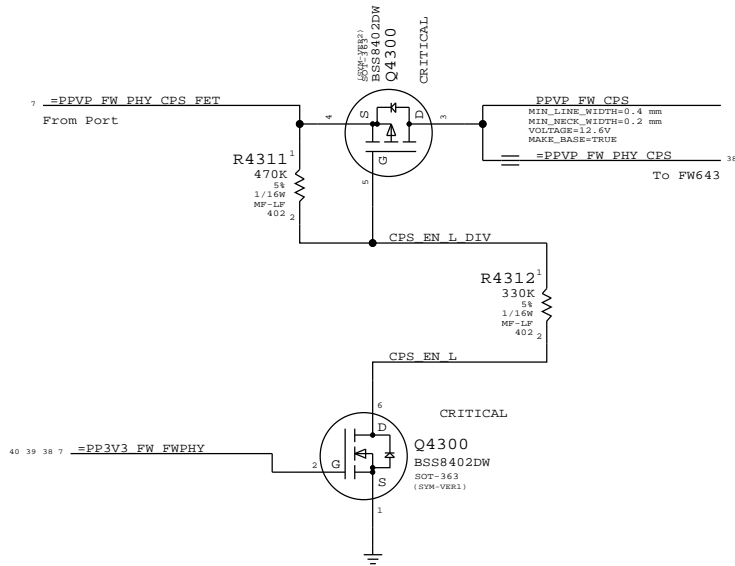
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)
1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

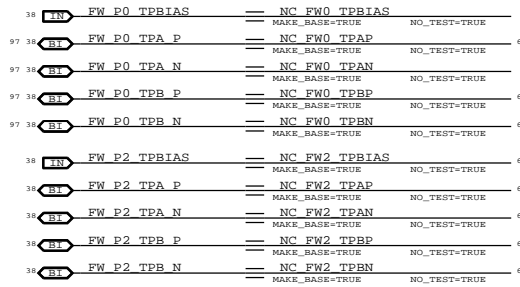
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



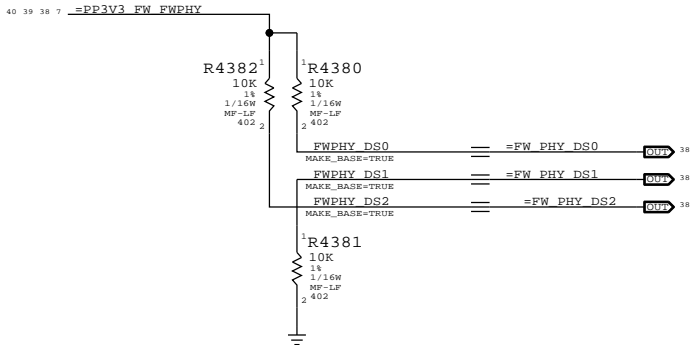
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



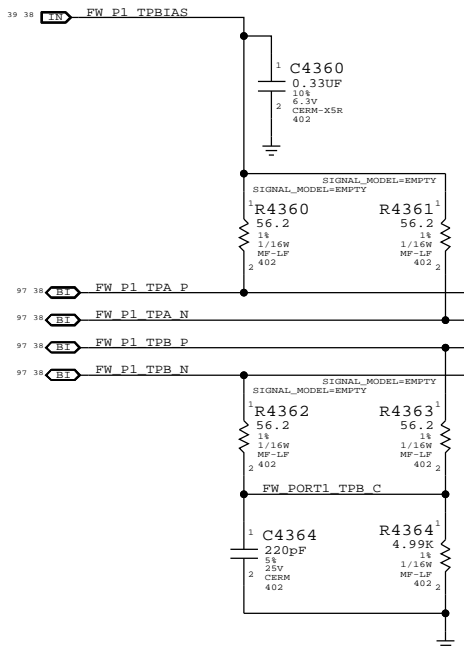
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



Termination

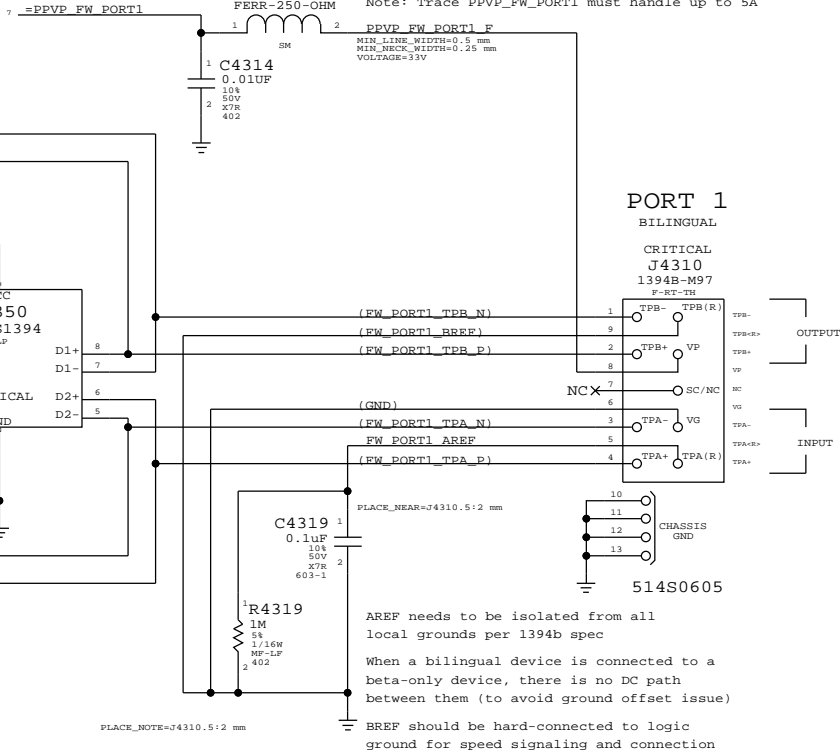
Place close to FireWire PHY



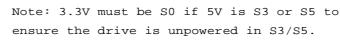
Cable Power

CRITICAL
L4310
FERR-250-OHM

Note: Trace PPVP_FW_PORT1 must handle up to 5A



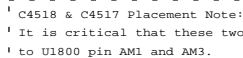
SYNC MASTER=T27 REF		SYNC DATE=06/10/2010	
PAGE TITLE		PAGE	
FireWire Connector		DRAWING NUMBER	051-9585
Apple Inc.		REVISION	3.0.0
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Notes:

OOBD2R was OOB_TEMP, from SSD, to SMC

OOBR2D was TEMP_CTL, from SMC, to SSD



Internally PD ~150K
Write:0xB6 Read:0xB7

Timing diagram for SATA HDD D2R P and N signals.

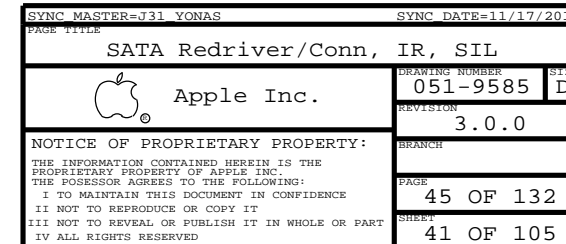
Parameters:

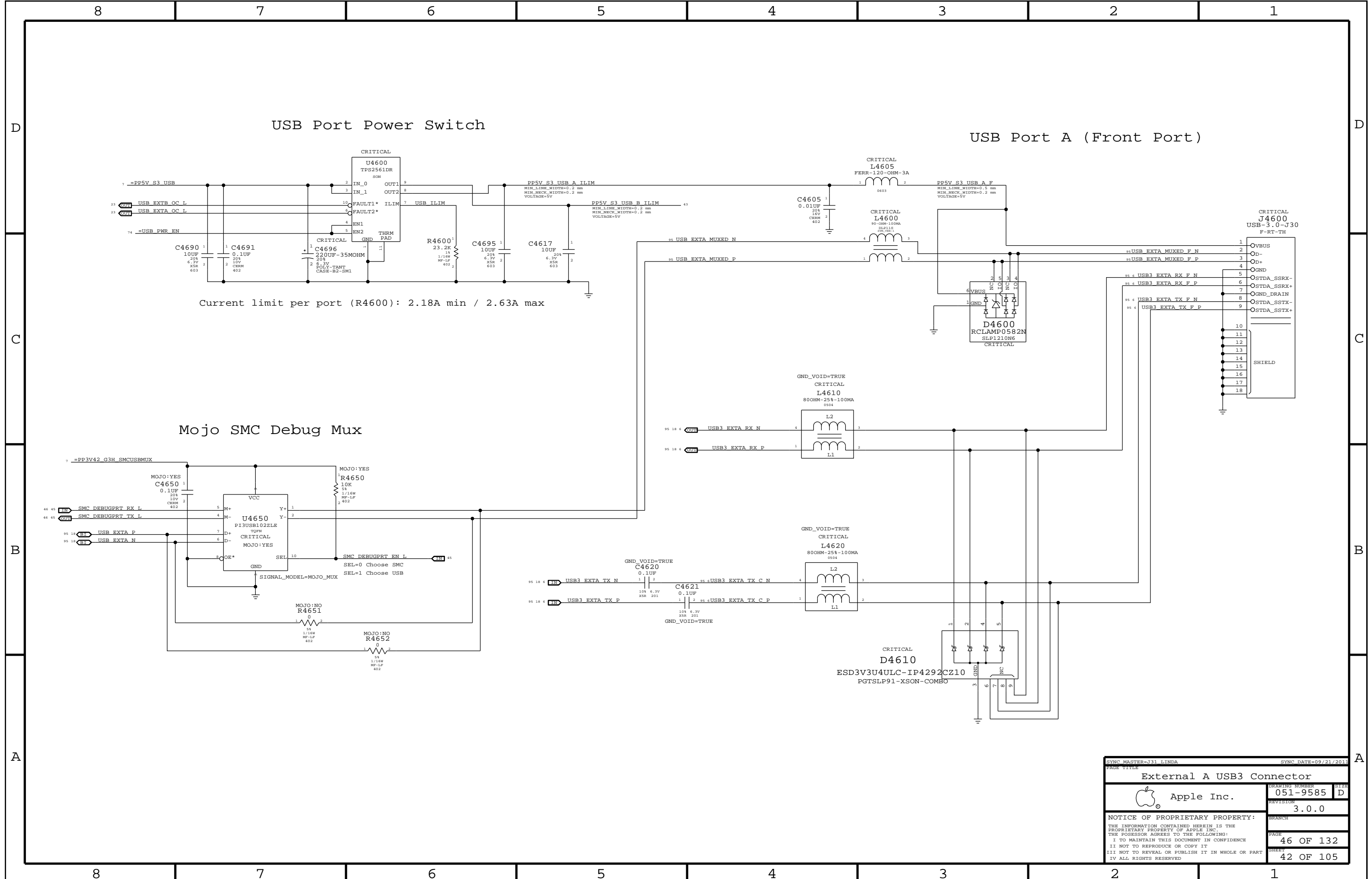
- PLACE_HEAR=01800.AM1:500M
- GND_V0ID=TRUE

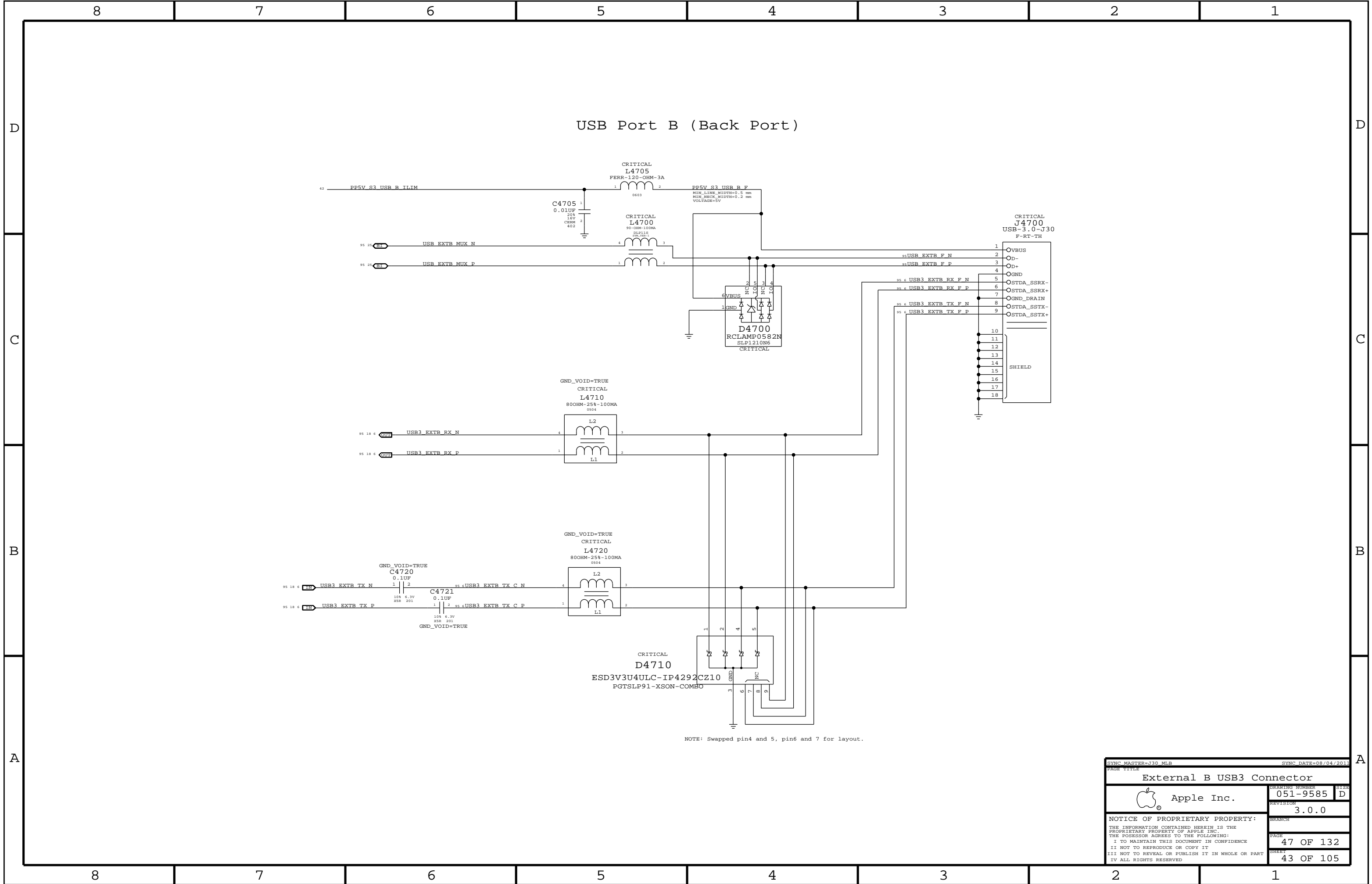
Waveform C4518 (SATA HDD D2R P) shows a signal that is high for most of the time, with a narrow pulse low at 10ns. The signal is labeled with a value of 16.95.


Waveform C4517 (SATA HDD D2R N) shows a signal that is high for most of the time, with a narrow pulse low at 10ns. The signal is labeled with a value of 16.95.

The diagram includes a time scale of 0.01UF.




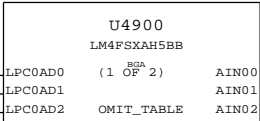





SYNC MASTER=J30_MLB		SYNC DATE=08/04/2011	
PAGE TITLE			
External B USB3 Connector			
 Apple Inc.		DRAWING NUMBER	051-9585
		SIZE	D
		REVISION	3.0.0
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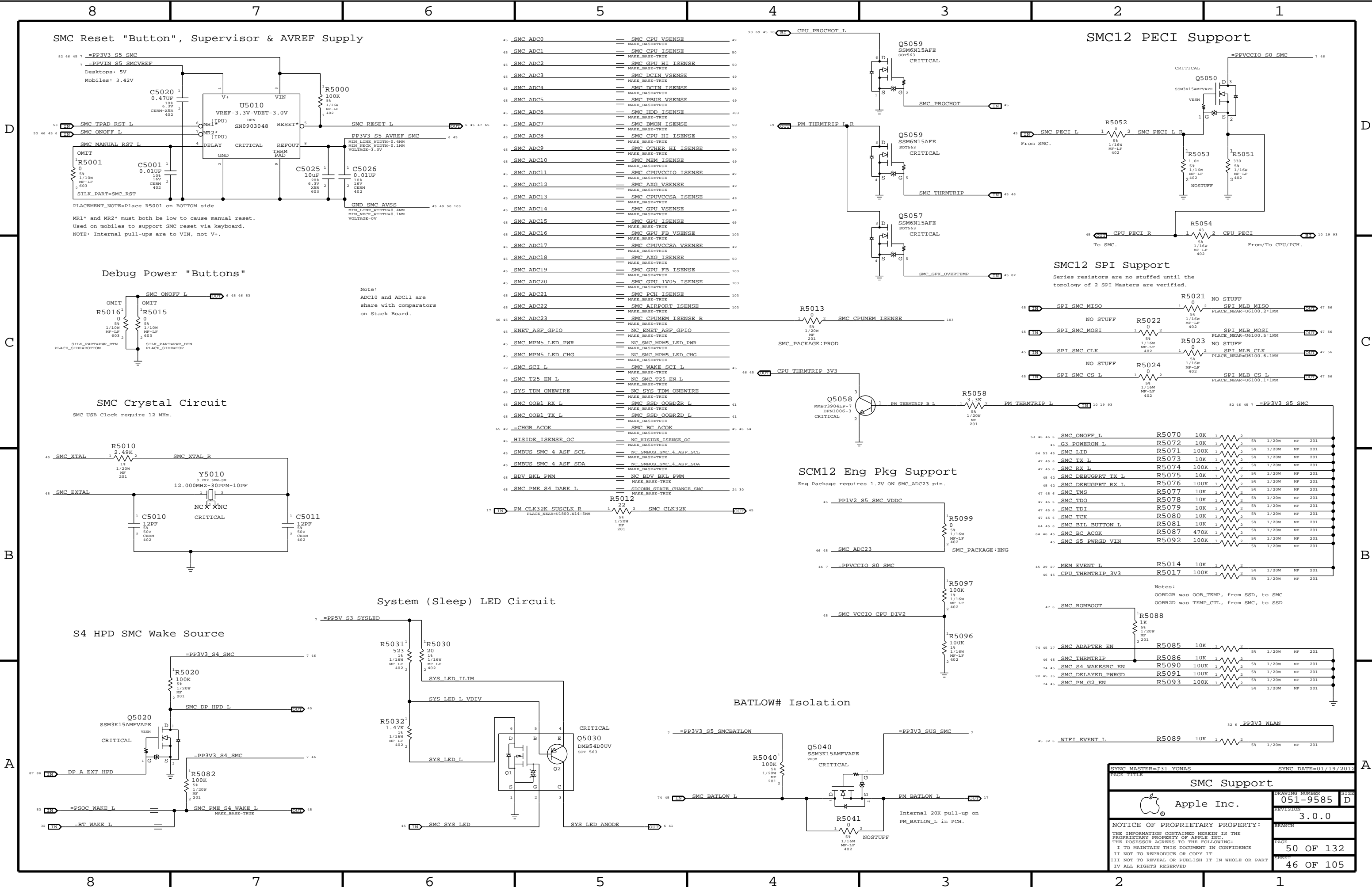
[illegible]


SYNC MASTER-K18 MLB		SYNC DATE=04/27/2010	
PAGE TITLE			
Front Flex Support			
 Apple Inc.		DRAWING NUMBER 051-9585	
		SIZE D	
		REVISION 3.0.0	
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		SHEET 44 OF 105	



NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=J31 YONAS		SYNC DATE=12/19/2011			
PAGE TITLE					
SMC					
	Apple Inc.	DRAWING NUMBER	051-9585	SIZE	D
		REVISION			
		3.0.0			
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SYNC MASTER=J31 YONAS		SYNC DATE=01/19/2012	
PAGE TITLE			
SMC Support			
 Apple Inc.		DRAWING NUMBER	051-9585
		REVISION	3.0.0
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D

C

B

A

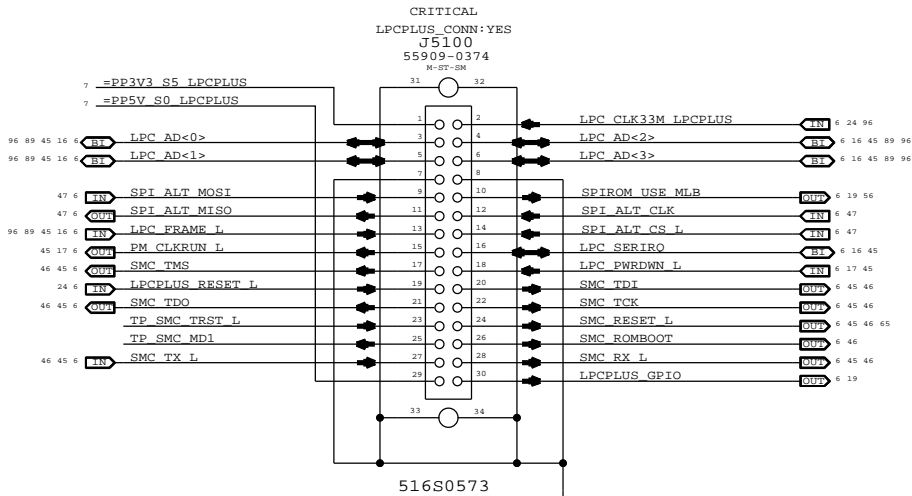
D

C

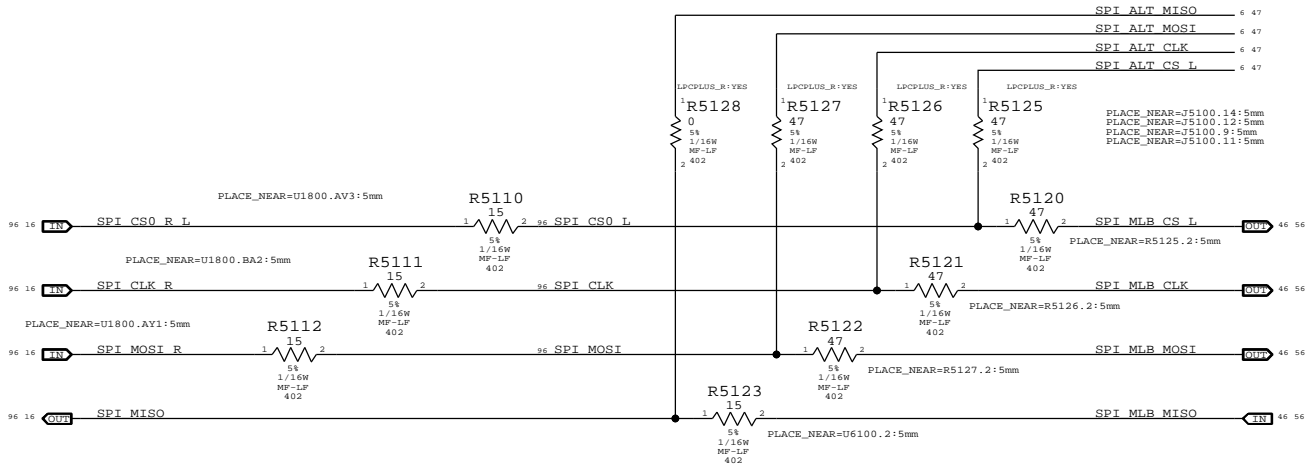
B


A

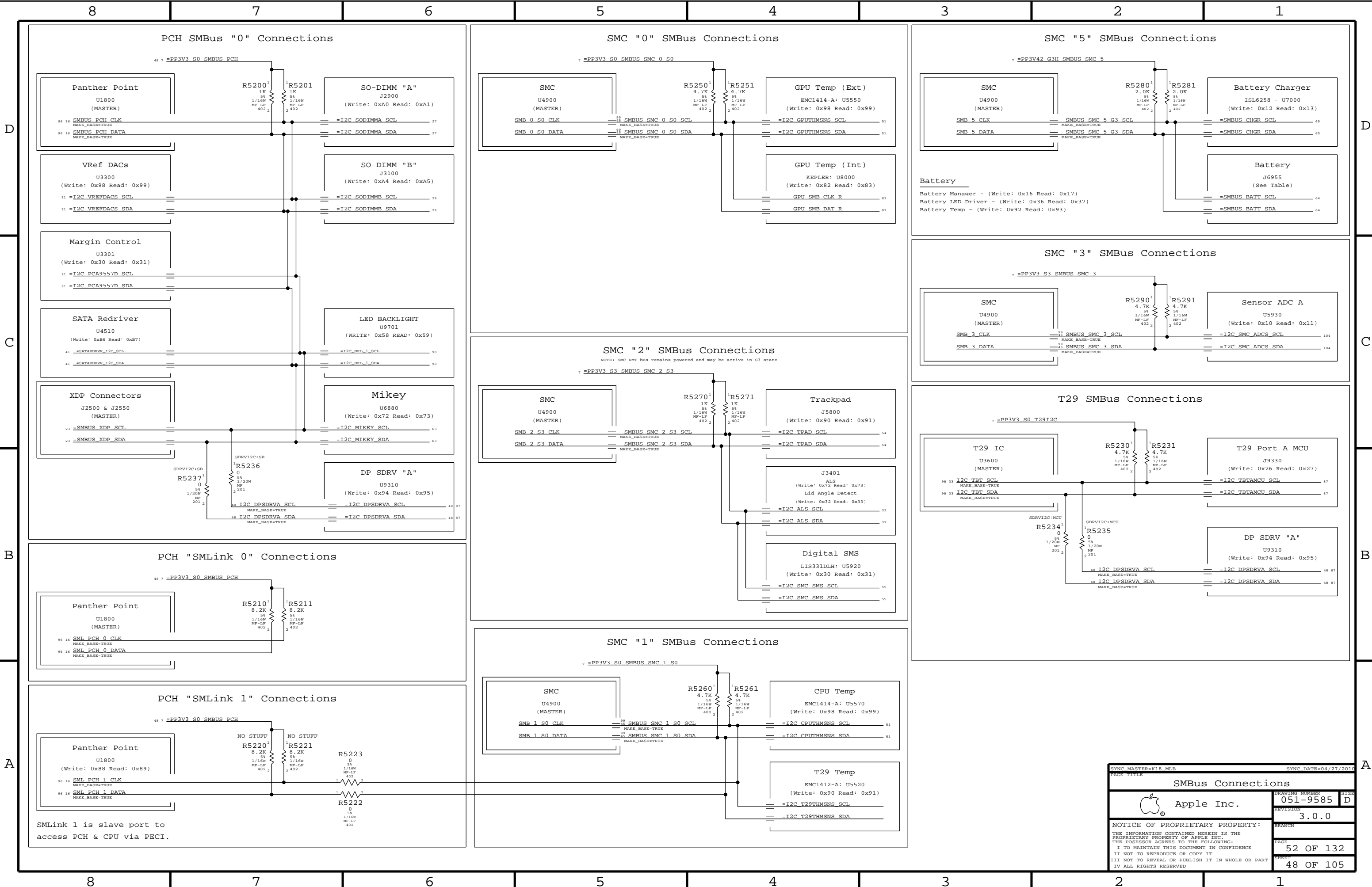
LPC+SPI Connector

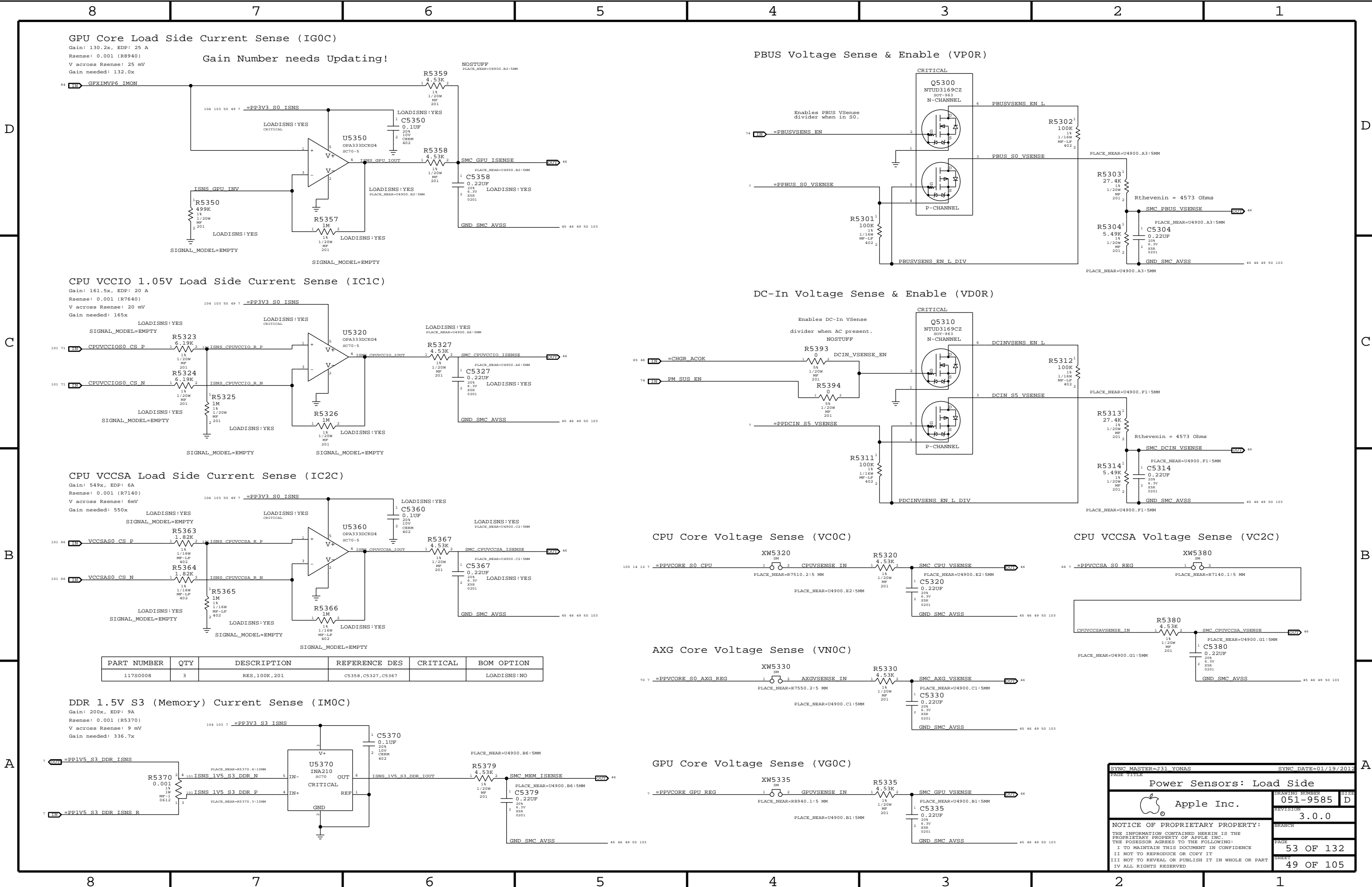


SPI Bus Series Termination



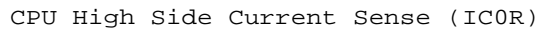
SYNC MASTER=J5 MLB		SYNC DATE=05/26/2011	
PAGE TITLE			
LPC+SPI Debug Connector			
	DRAWING NUMBER		SIZE
	051-9585		D
Apple Inc.		REVISION	
		3.0.0	
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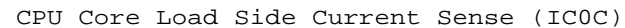
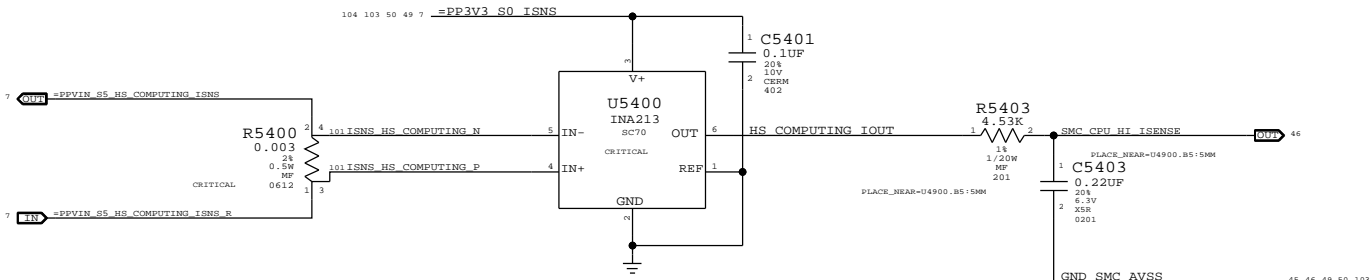


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,100K,201	C5358,C5327,C5367		LOADISNS:NO

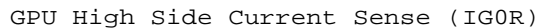
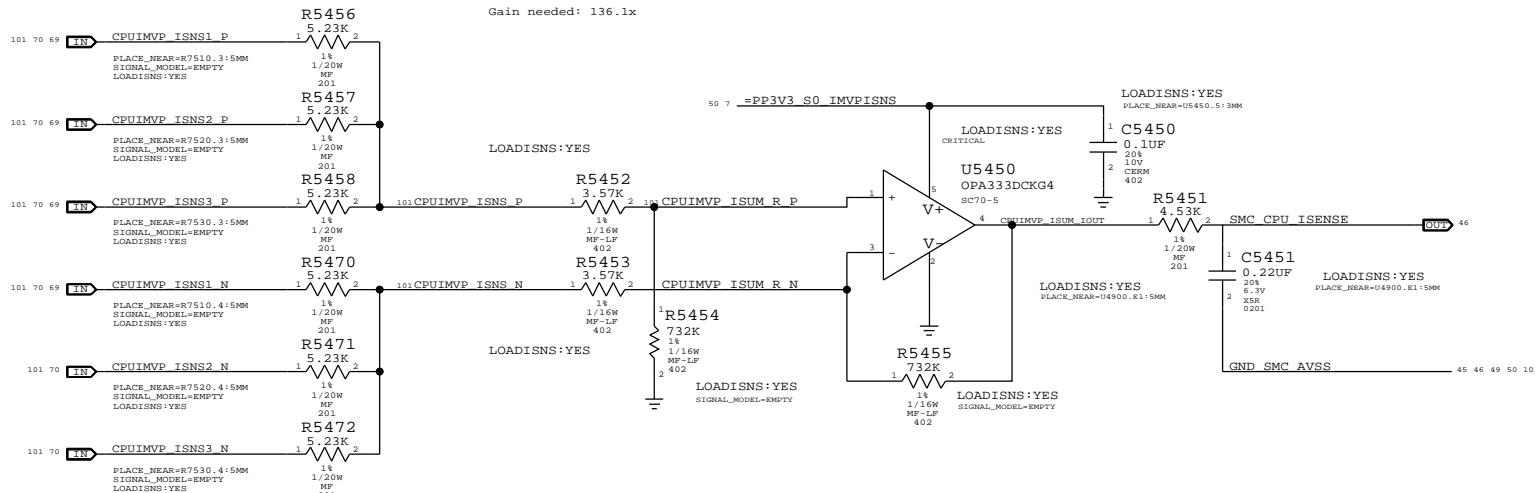
SYNC MASTER=J31 YONAS		SYNC DATE=01/19/2012	
PAGE TITLE		Power Sensors: Load Side	
		DRAWING NUMBER	051-9585
		REVISION	3.0.0
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		PAGE	53 OF 132
		SHEET	49 OF 105



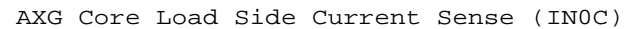
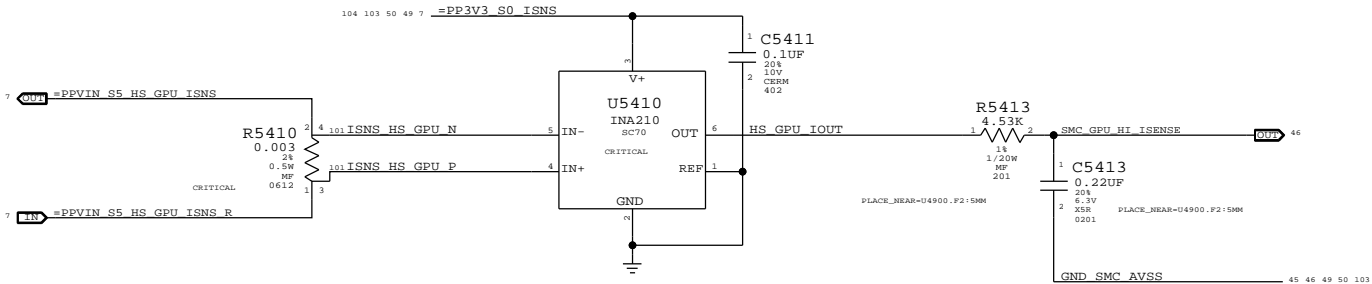
Gain: 50x, EDP: 22.8 A
Rsense: 0.003 (R5400)
V across Rsense: 68.4 mV
Gain needed: 48.25x



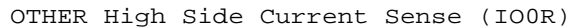
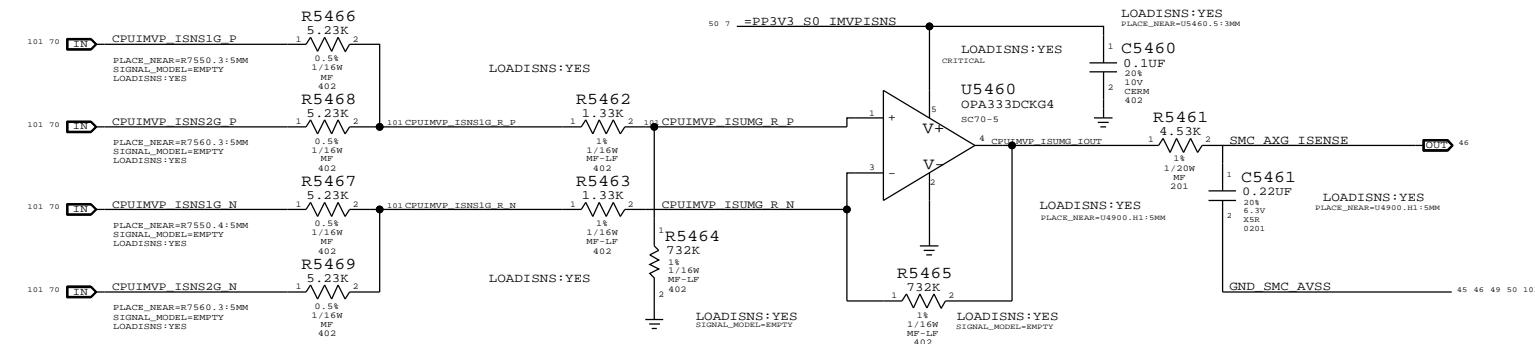
```
Gain: 136.1x, EDP: 97 A
Rsense: 3x of 0.00075 (R7510, R7520, R7530), Rsum: 0.00025.
V across Rsense: 24.25 mV
Gain needed: 136.1x
```



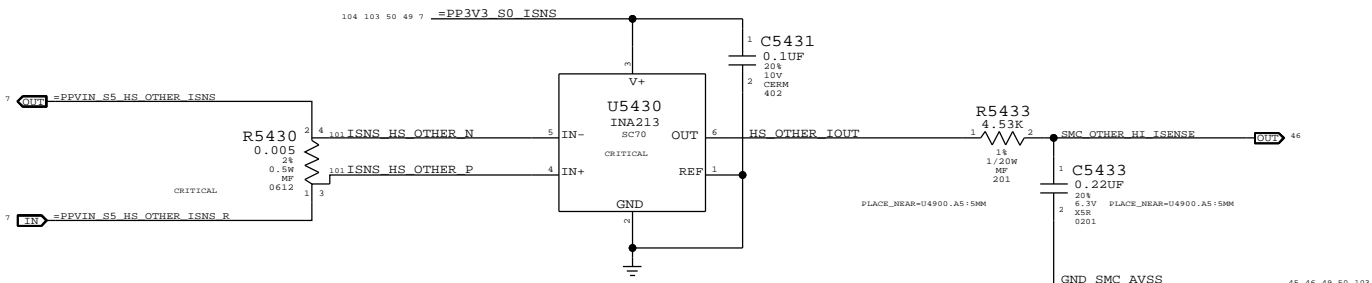
Gain: 200x, EDP: 5.2 A (Kepler)
Rsense: 0.003 (R5410)
V across Rsense: 15.6 mV
Gain needed: 211.54x (Kepler)



Gain: 185.5x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375.
V across Rsense: 17.25 mV
Gain needed: 191.3x



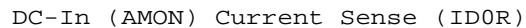
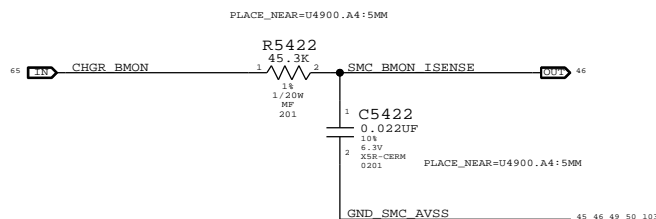
Gain: 50x, EDP: 10.3 A
Rsense: 0.005 (R5440)
V across Rsense: 51.5 mV
Gain needed: 64.1x



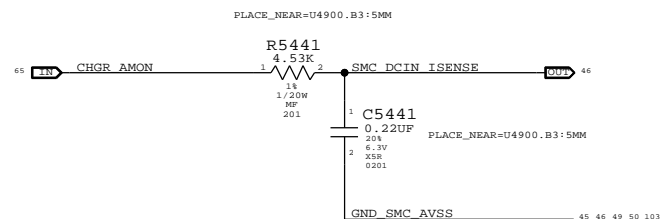
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,100K,201	C5451,C5461		LOADISNS:NO




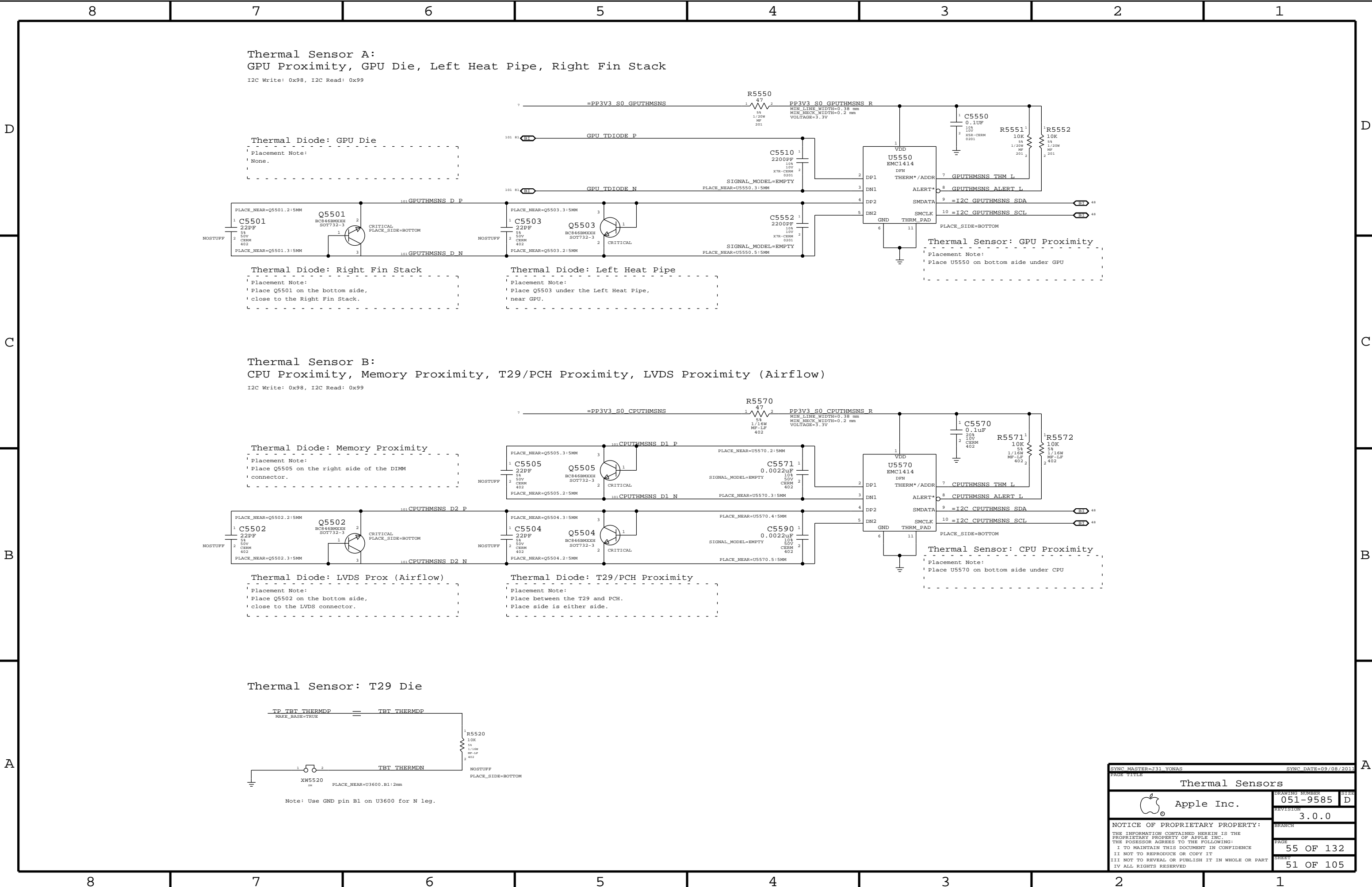
Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Measured I: 9.2 A



Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Measured I: 8.3 A



SYNC MASTER=J31 YONAS		SYNC DATE=10/25/2011	
PAGE TITLE			
Power Sensors: High Side, CPU, AXG			
	Apple Inc.		DRAWING NUMBER 051-9585
			SIZE D
			REVISION 3.0.0
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Thermal Sensor A:
GPU Proximity, GPU Die, Left Heat Pipe, Right Fin Stack
I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: GPU Die
Placement Note:
None.

Thermal Diode: Right Fin Stack
Placement Note:
Place Q5501 on the bottom side,
close to the Right Fin Stack.

Thermal Diode: Left Heat Pipe
Placement Note:
Place Q5503 under the Left Heat Pipe,
near GPU.

Thermal Sensor: GPU Proximity
Placement Note:
Place U5550 on bottom side under GPU

Thermal Sensor B:
CPU Proximity, Memory Proximity, T29/PCH Proximity, LVDS Proximity (Airflow)
I2C Write: 0x98, I2C Read: 0x99

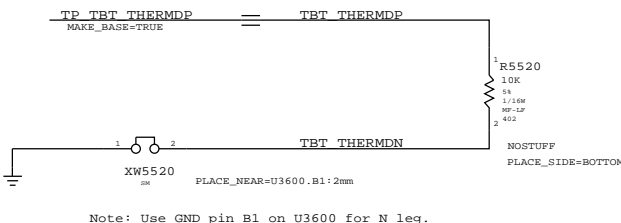
Thermal Diode: Memory Proximity
Placement Note:
Place Q5505 on the right side of the DIMM
connector.

Thermal Diode: LVDS Prox (Airflow)
Placement Note:
Place Q5502 on the bottom side,
close to the LVDS connector.


Thermal Diode: T29/PCH Proximity
Placement Note:
Place between the T29 and PCH.
Place side is either side.

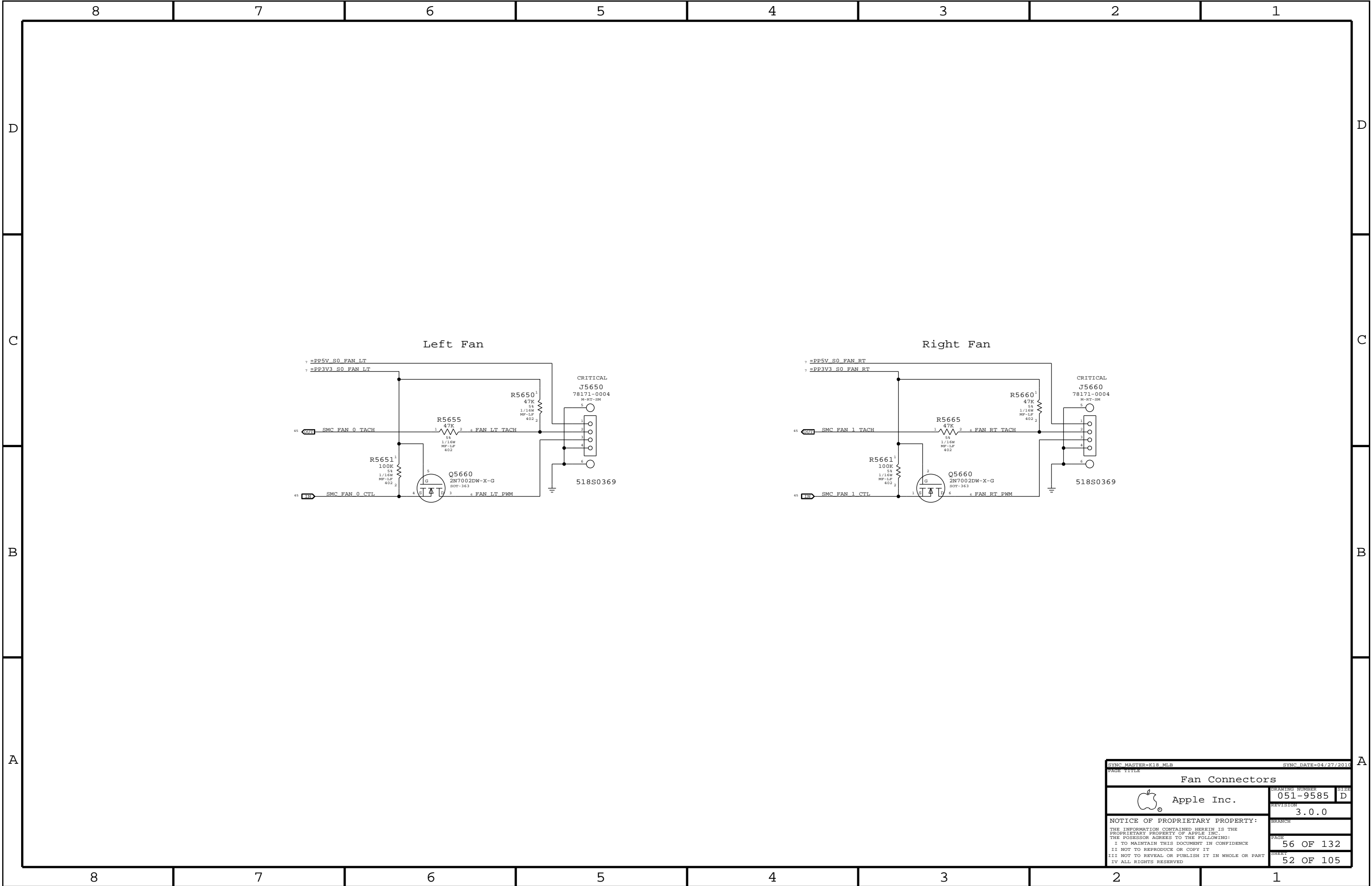
Thermal Sensor: CPU Proximity
Placement Note:
Place U5570 on bottom side under CPU

Thermal Sensor: T29 Die

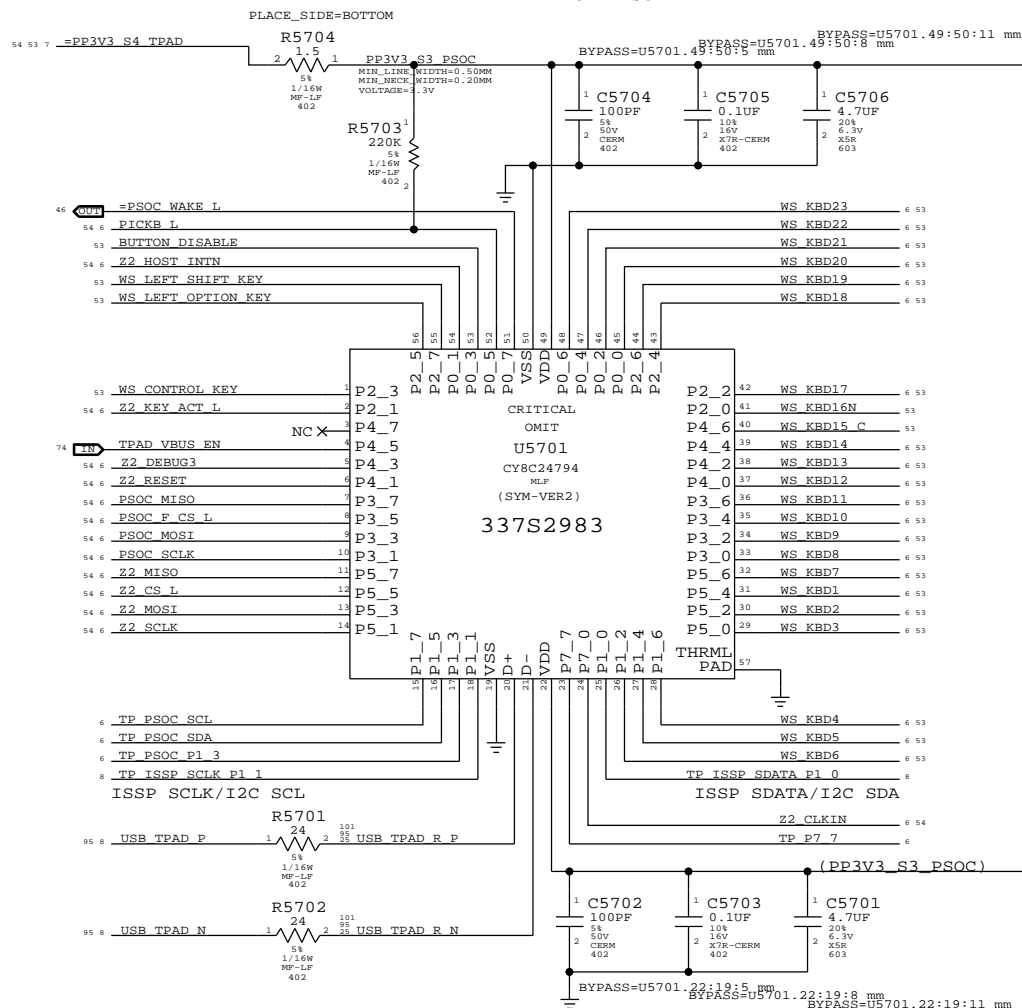


Note: Use GND pin B1 on U3600 for N leg.

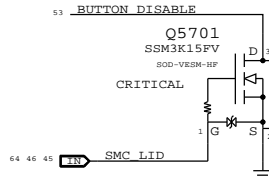
SYNC MASTER=J31 YONAS		SYNC DATE=09/08/2011	
PAGE TITLE			
Thermal Sensors			
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- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB



```

THE TPAD BUTTONS WILL BE DISABLED
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

```

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A 800A	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60mA (MAX) 60mA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8mA (TYP) 14mA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4mA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

54 53 7 =PP3V3 S4 TPAD NCX 32

53 7 =PP3V42 G3H TPAD 30

53 6 WS KBD1 29

53 6 WS KBD2 28

53 6 WS KBD3 27

53 6 WS KBD4 26

53 6 WS KBD5 25

53 6 WS KBD6 24

53 6 WS KBD7 23

53 6 WS KBD8 22

53 6 WS KBD9 21

53 6 WS KBD10 20

53 6 WS KBD11 19

53 6 WS KBD12 18

53 6 WS KBD13 17

53 6 WS KBD14 16

53 6 WS KBD15 CAP 15

6 WS KBD15 CAP 14

6 WS KBD16 NUM 13

53 6 WS KBD17 12

53 6 WS KBD18 11

53 6 WS KBD19 10

53 6 WS KBD20 9

53 6 WS KBD21 8

53 6 WS KBD22 7

53 6 WS KBD23 6

6 WS KBD ONOFF L 5

53 6 WS LEFT SHIFT KBD 3

53 6 WS LEFT OPTION KBD 2

53 6 WS CONTROL KBD 1

NCX 31

F=RT-20M

FF14-30A-R11B-B-3H

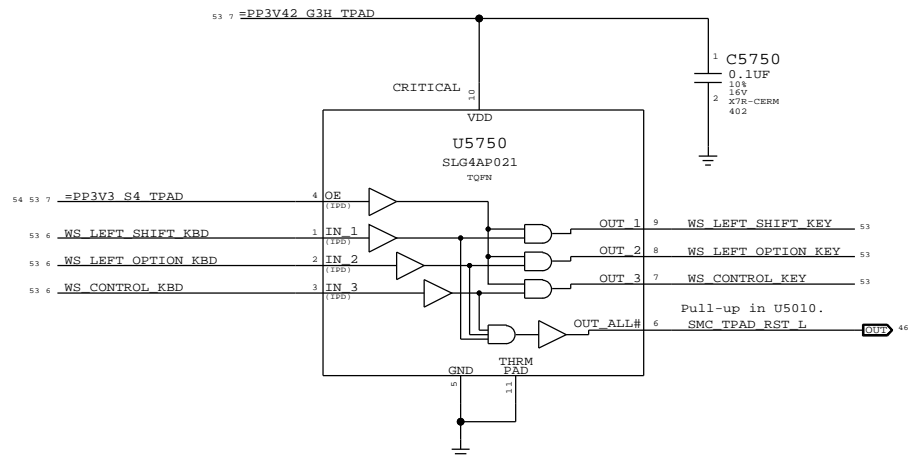
J5713


CRITICAL

518S0637

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).

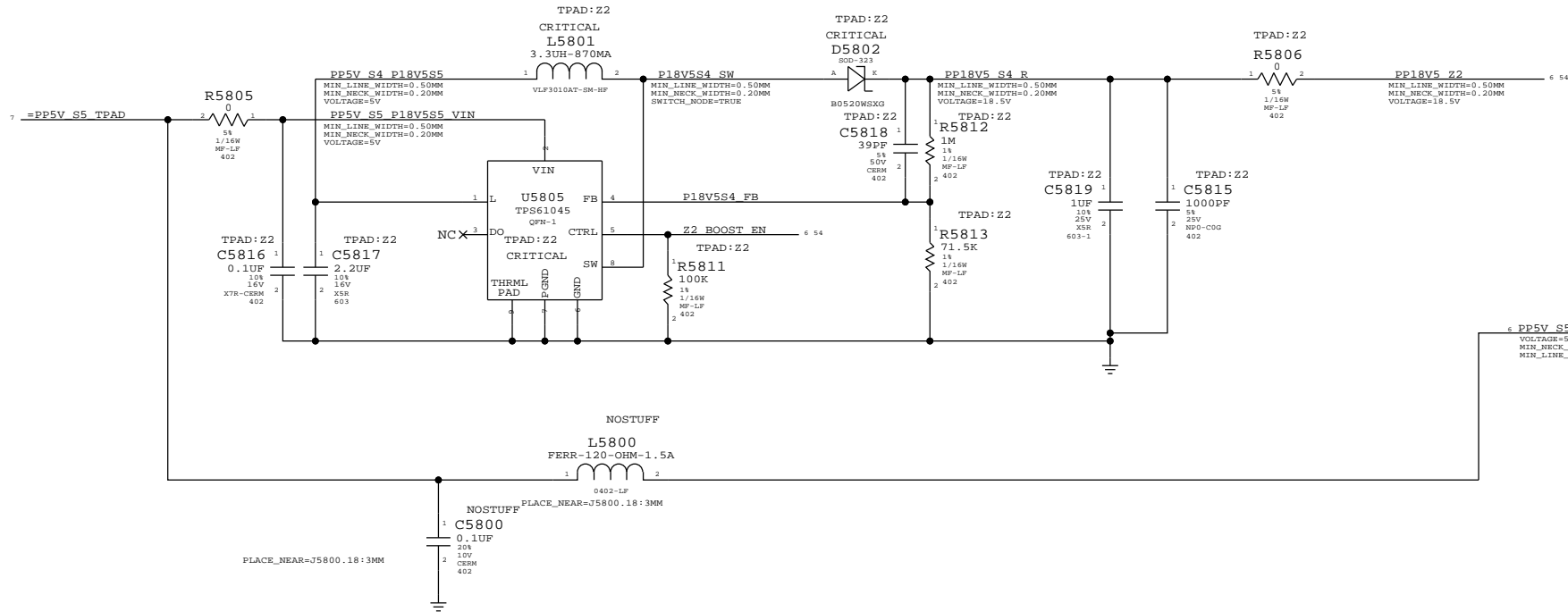


SYNC MASTER=J30 MLE		SYNC DATE=06/10/2011	
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WELLSPRING 1			
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		BRANCH	
		PAGE	
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		SHEET	
		53 OF 105	

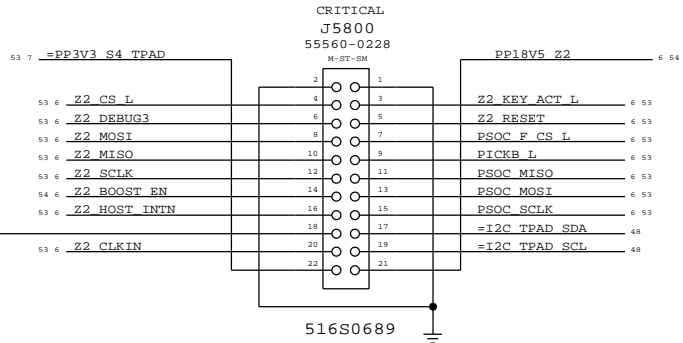
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:

- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

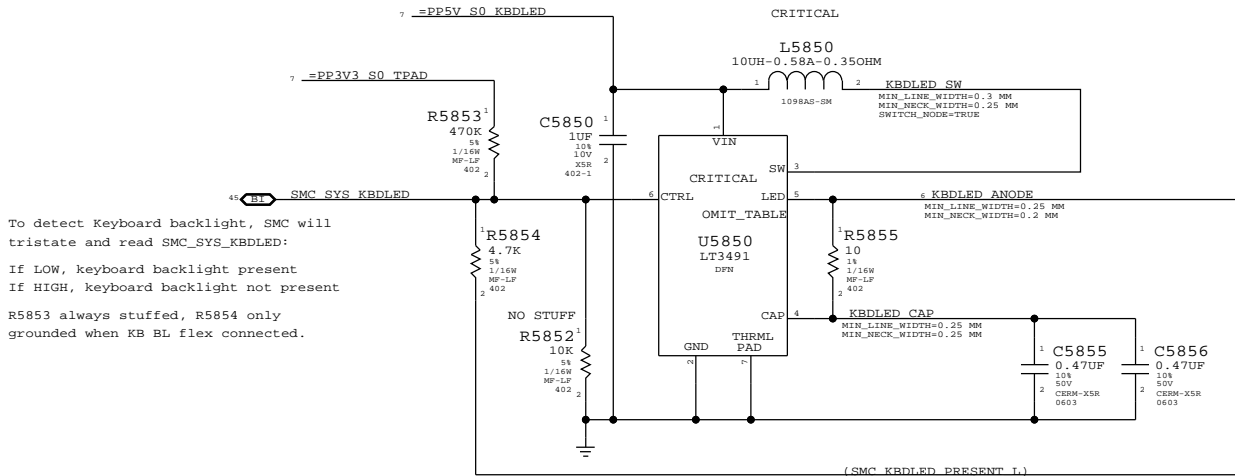


IPD Flex Connector



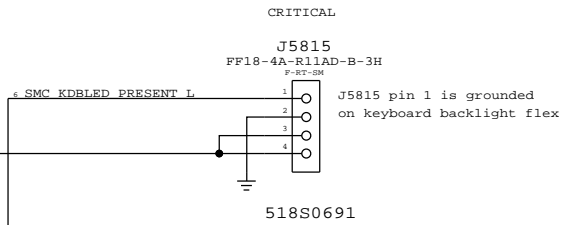
PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

Keyboard Backlight Driver & Detection




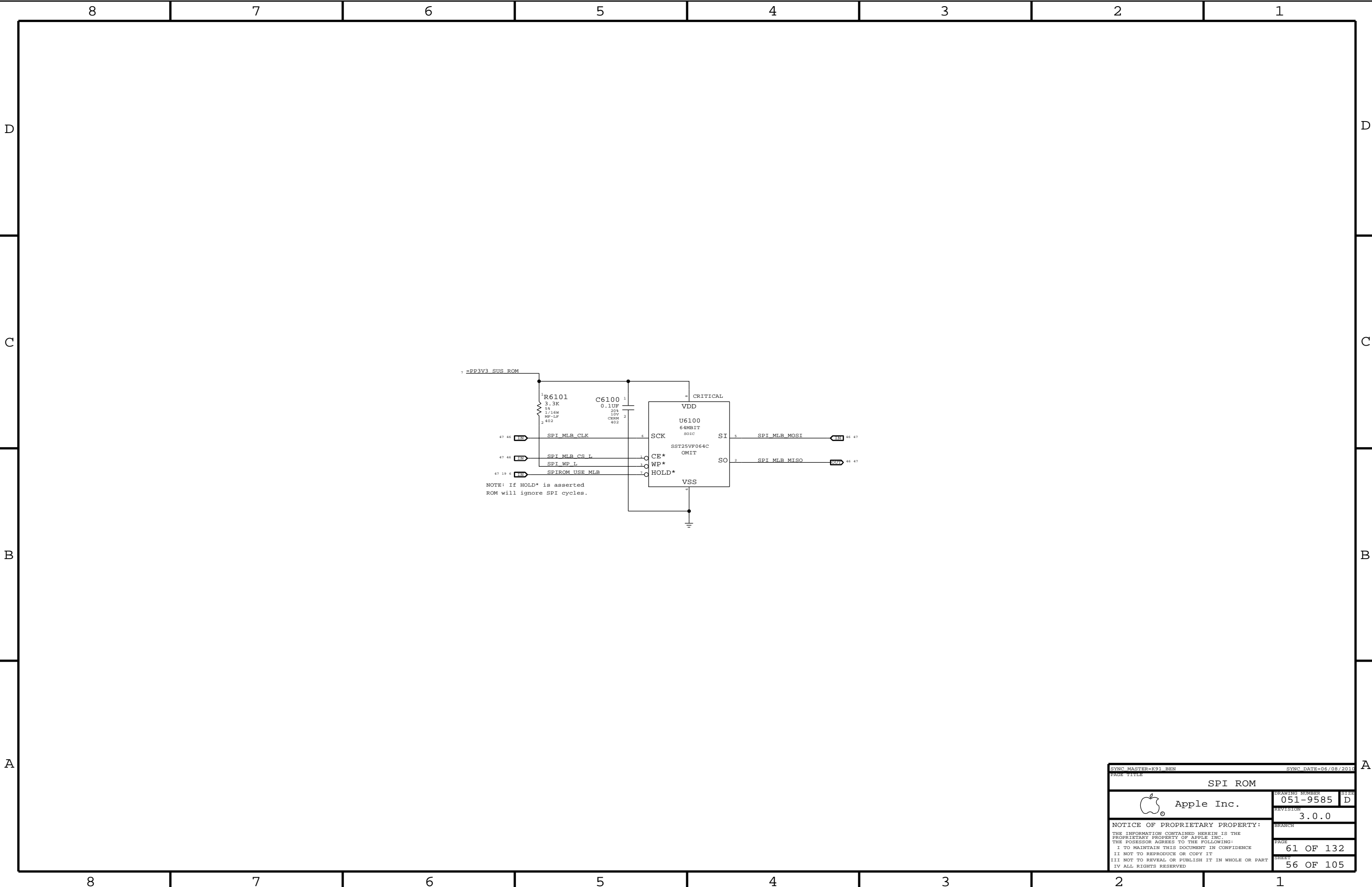
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
35383085	1	BT, BT422, 1-070100 LMD DRIVER, 0220PW-6	US850	CRITICAL	

SYNC MASTER=J31 LINDA		SYNC DATE=07/01/2013	
PAGE TITLE			
WELLSPRING 2			
 Apple Inc.		DRAWING NUMBER	051-9585
		REVISION	3.0.0
		BRANCH	
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		PAGE	58 OF 132
		SHEET	54 OF 105



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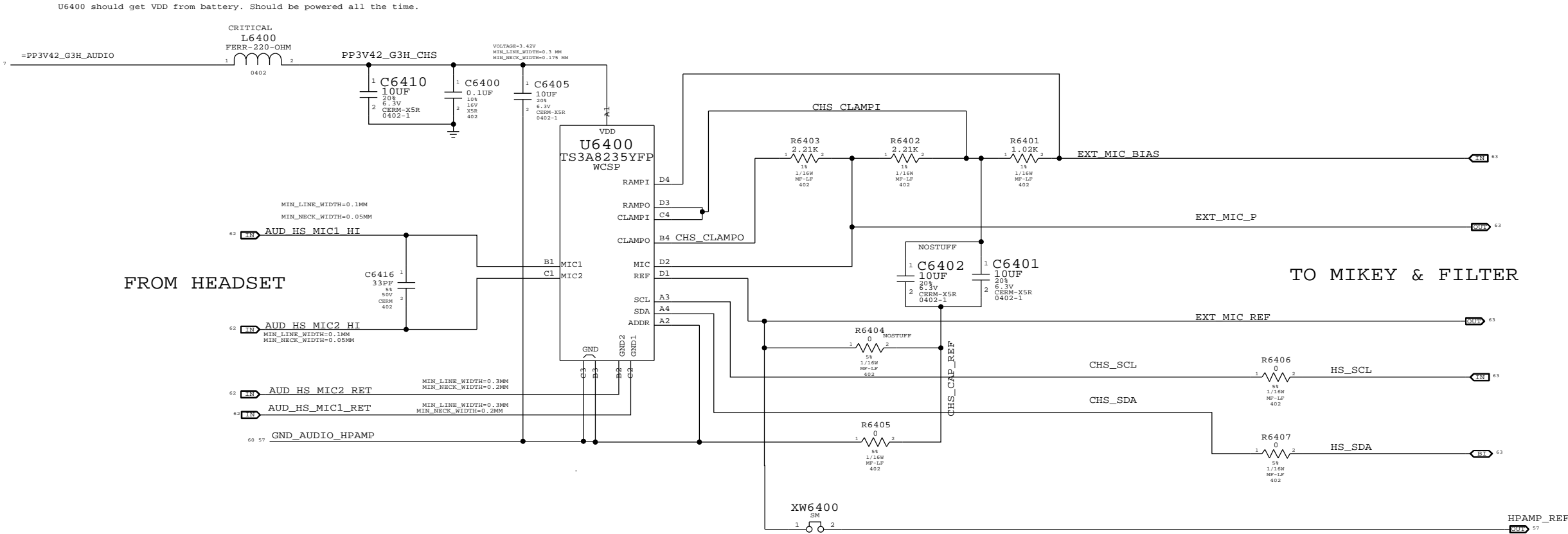
C

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A

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY


APN: 353S3066 as of July 2011

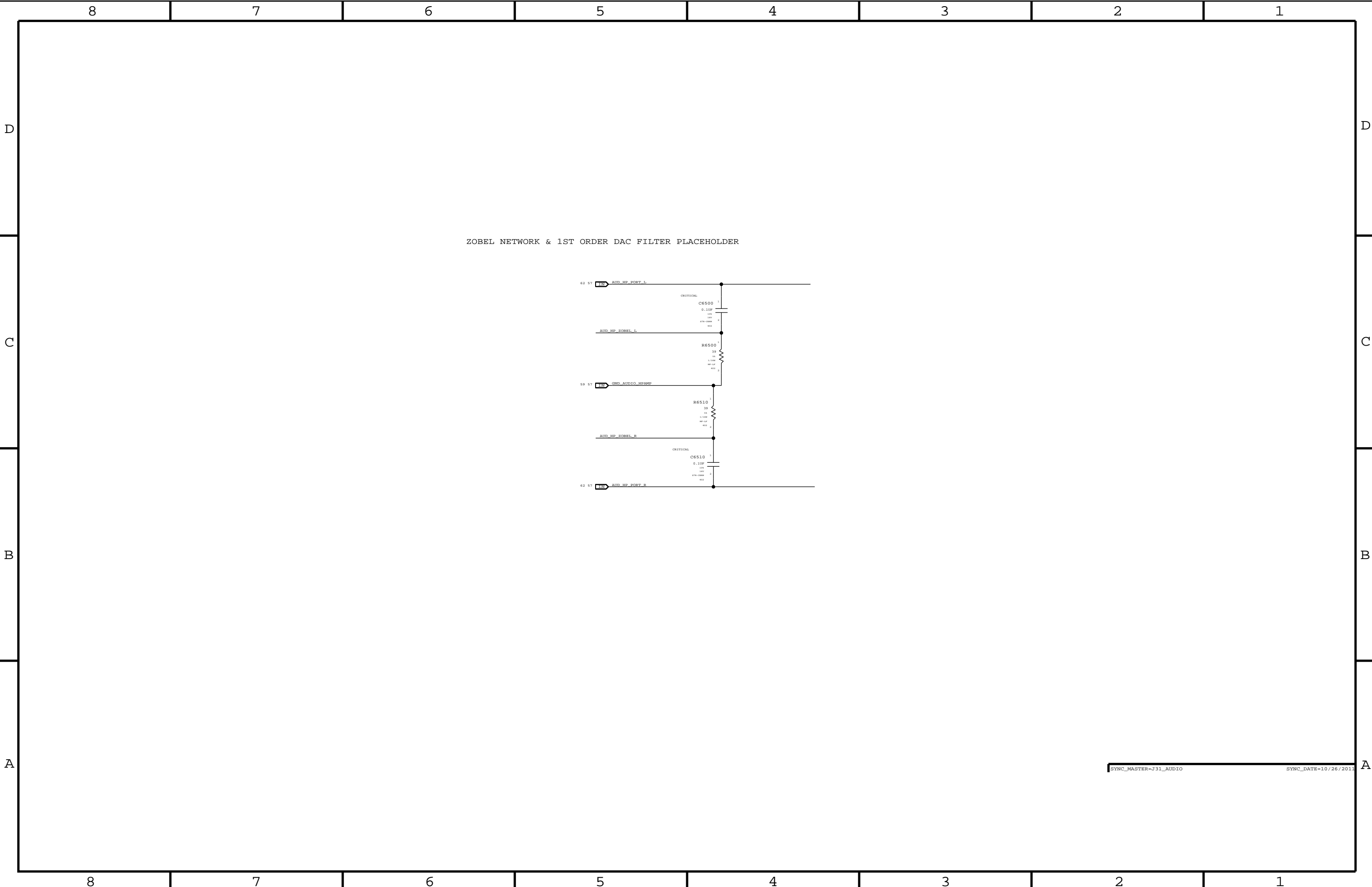


I2C ADDRESSES: CHS uses SMBus 0 connections

CHS U6400 READ 0111 0111 0x77

CHS U6400 WRITE 0111 0110 0x76

SYNC MASTER=J31 AUDIO		SYNC DATE=10/26/2011	
PAGE TITLE			
AUDIO: DETECT/MIC BIAS			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9585		D
		REVISION	
		3.0.0	
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		BRANCH	
		PAGE	64 OF 132
		SHEET	59 OF 105



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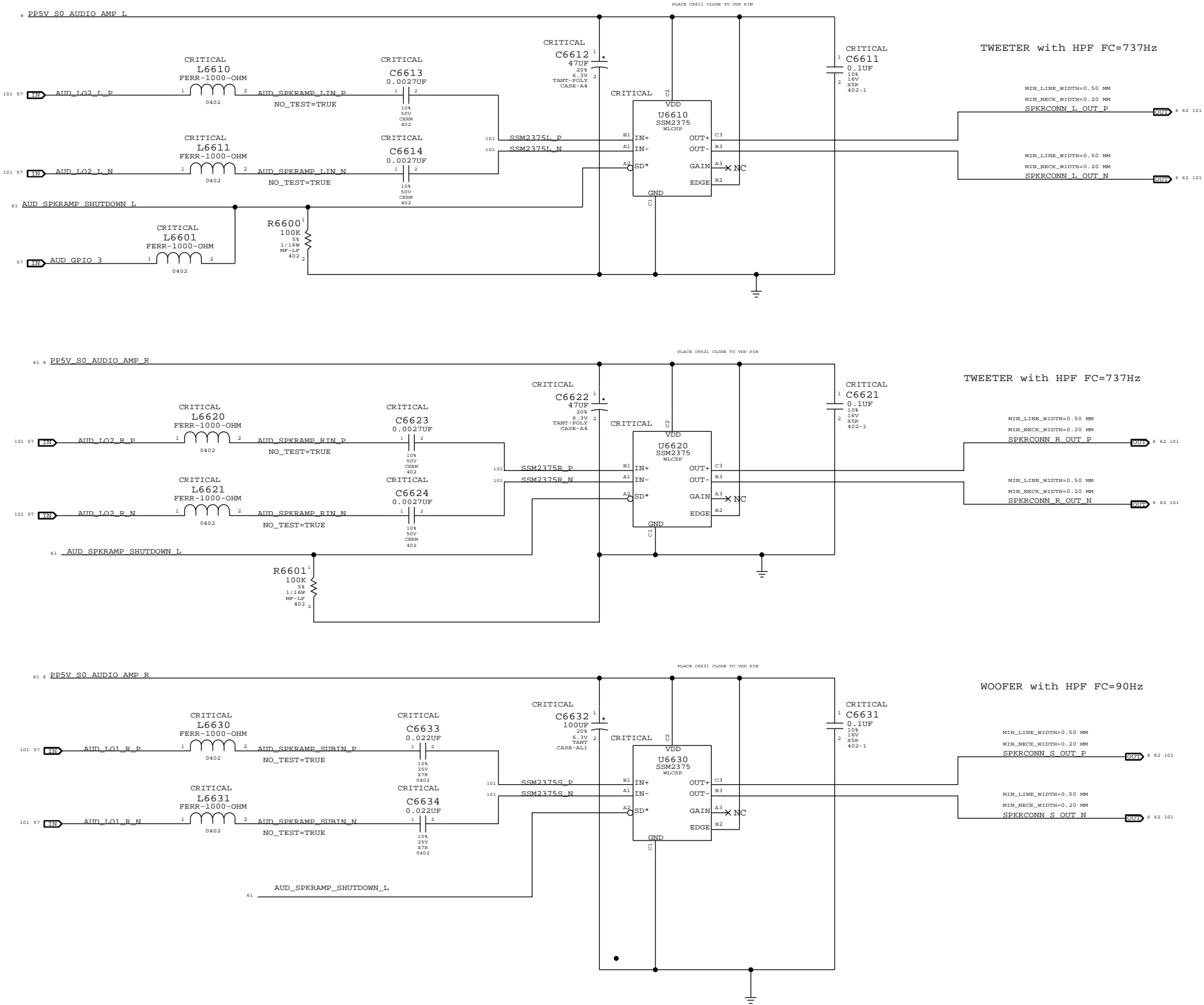
C


B

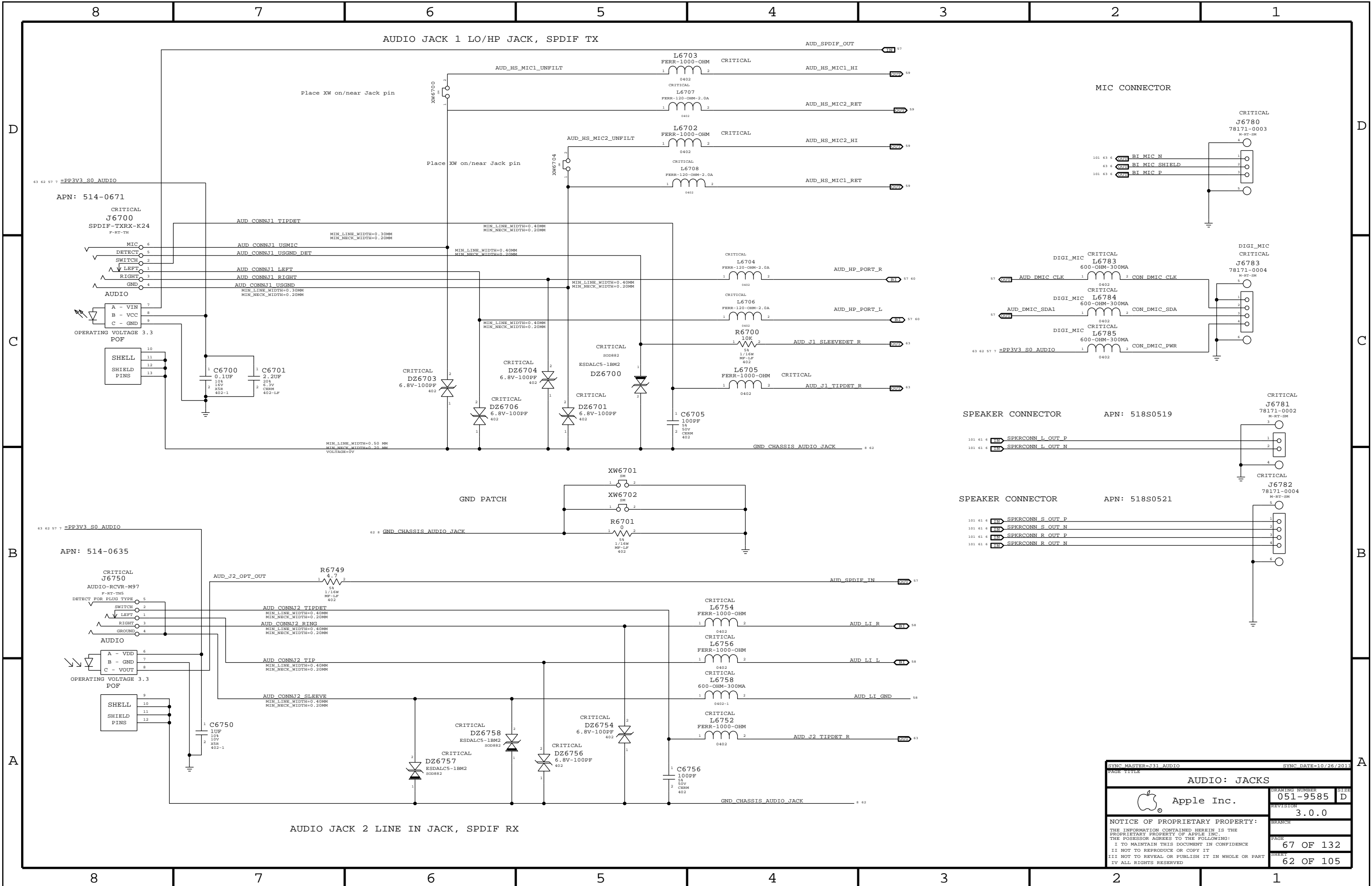
A


3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958 as of July 2011
GAIN = +3 DB Rin=80k irrespective of gain
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ

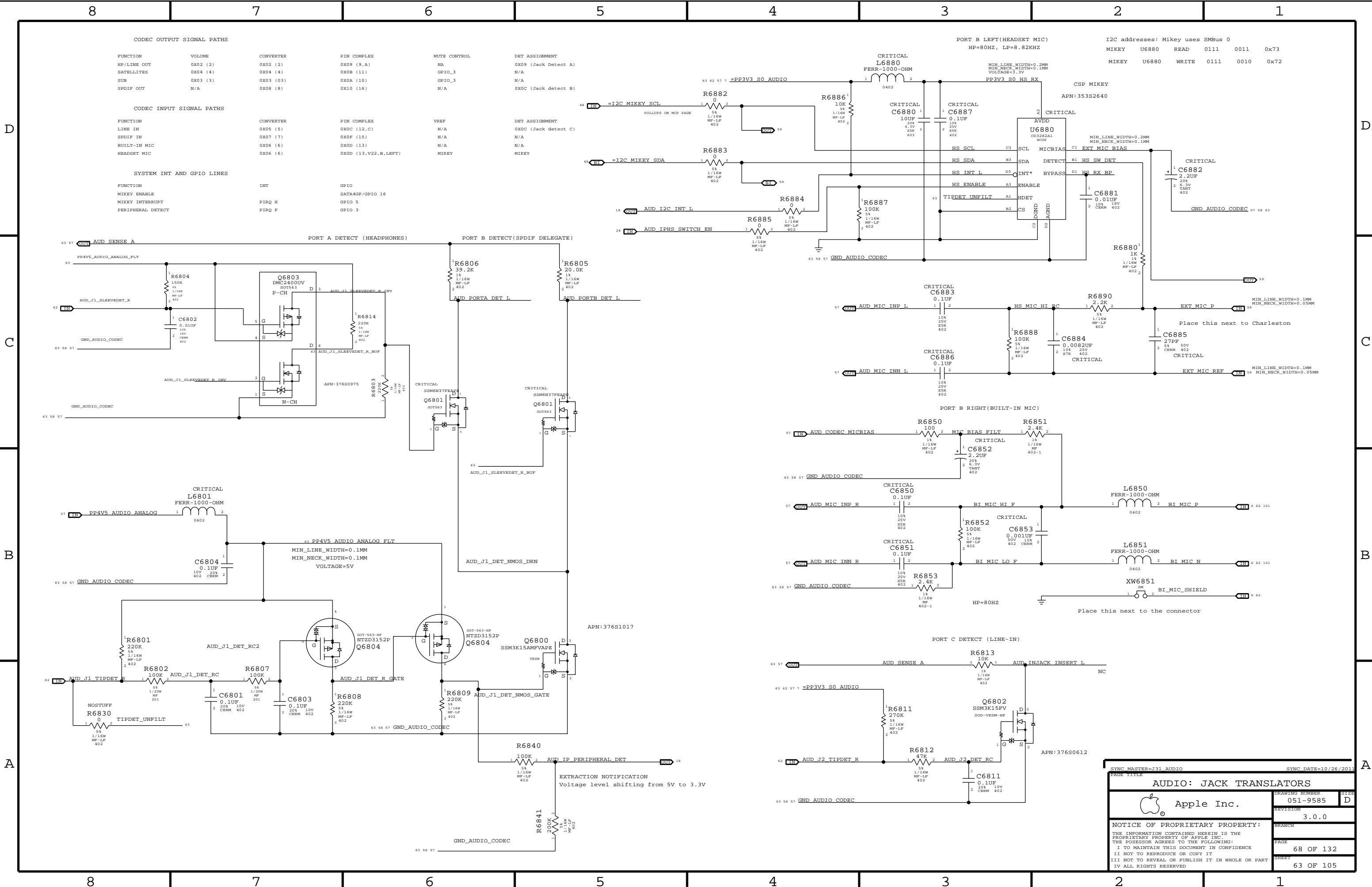
Gain Pin	Gain dB
Connect to VDD	6
Connect to VDD through 47k	12
Not connected	3
Connect to GND through 47k	9
Connect to GND	0




SYNC MASTER=J31 AUDIO		SYNC DATE=10/26/2011	
PAGE TITLE			
AUDIO: SPEAKER AMP			
	DRAWING NUMBER		DRAWING SIZE
	051-9585		D
	REVISION		3.0.0
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BRANCH		PAGE	
		66 OF 132	
SHEET		61 OF 105	

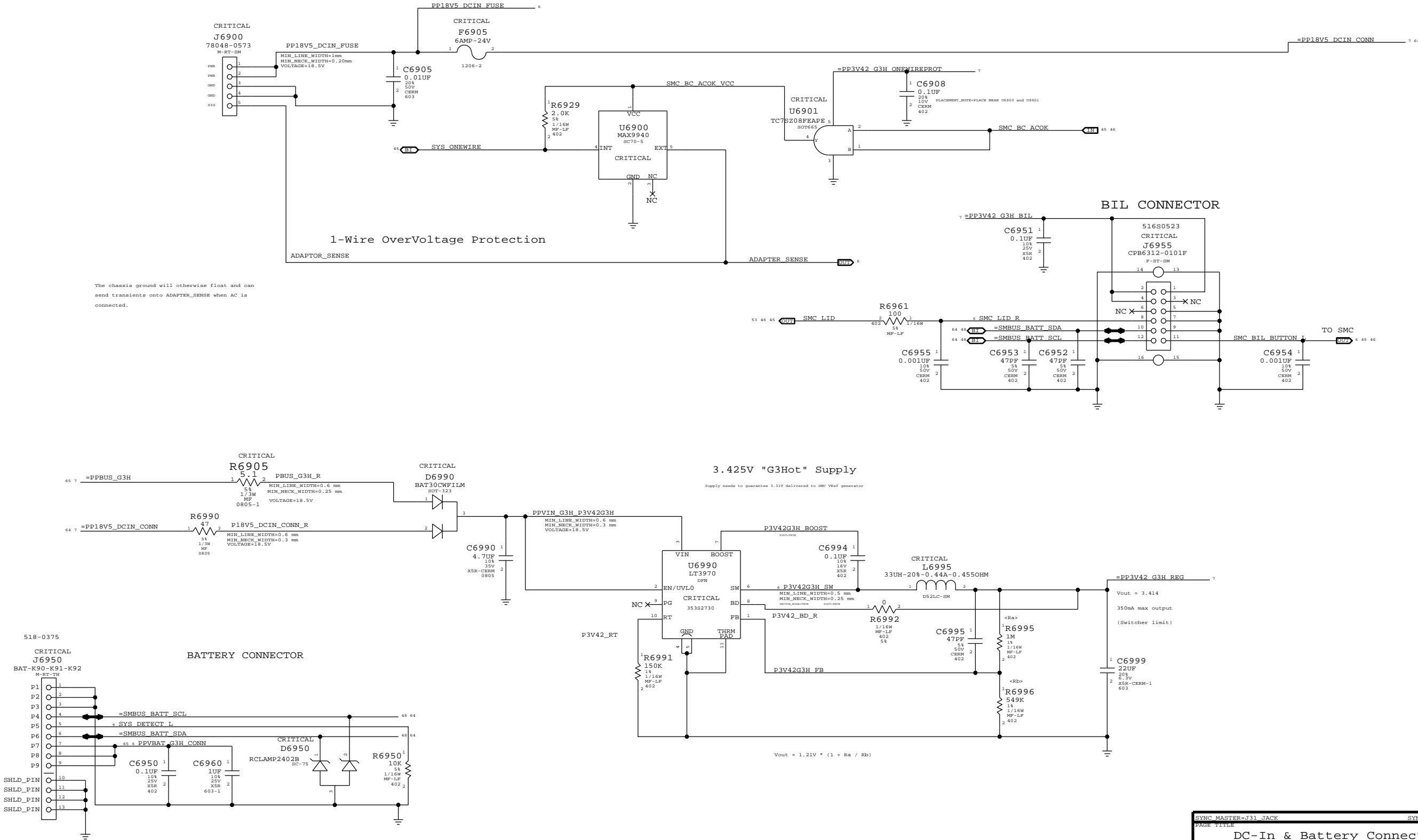



SYNC MASTER=J31 AUDIO		SYNC DATE=10/26/2011	
PAGE TITLE			
AUDIO: JACKS			
 Apple Inc.	DRAWING NUMBER	051-9585	SIZE D
	REVISION	3.0.0	
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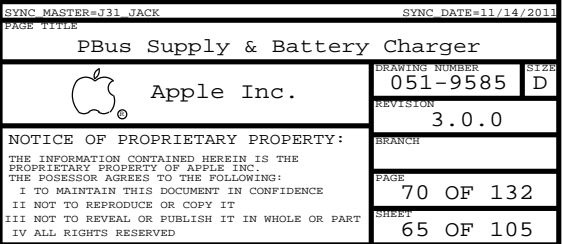


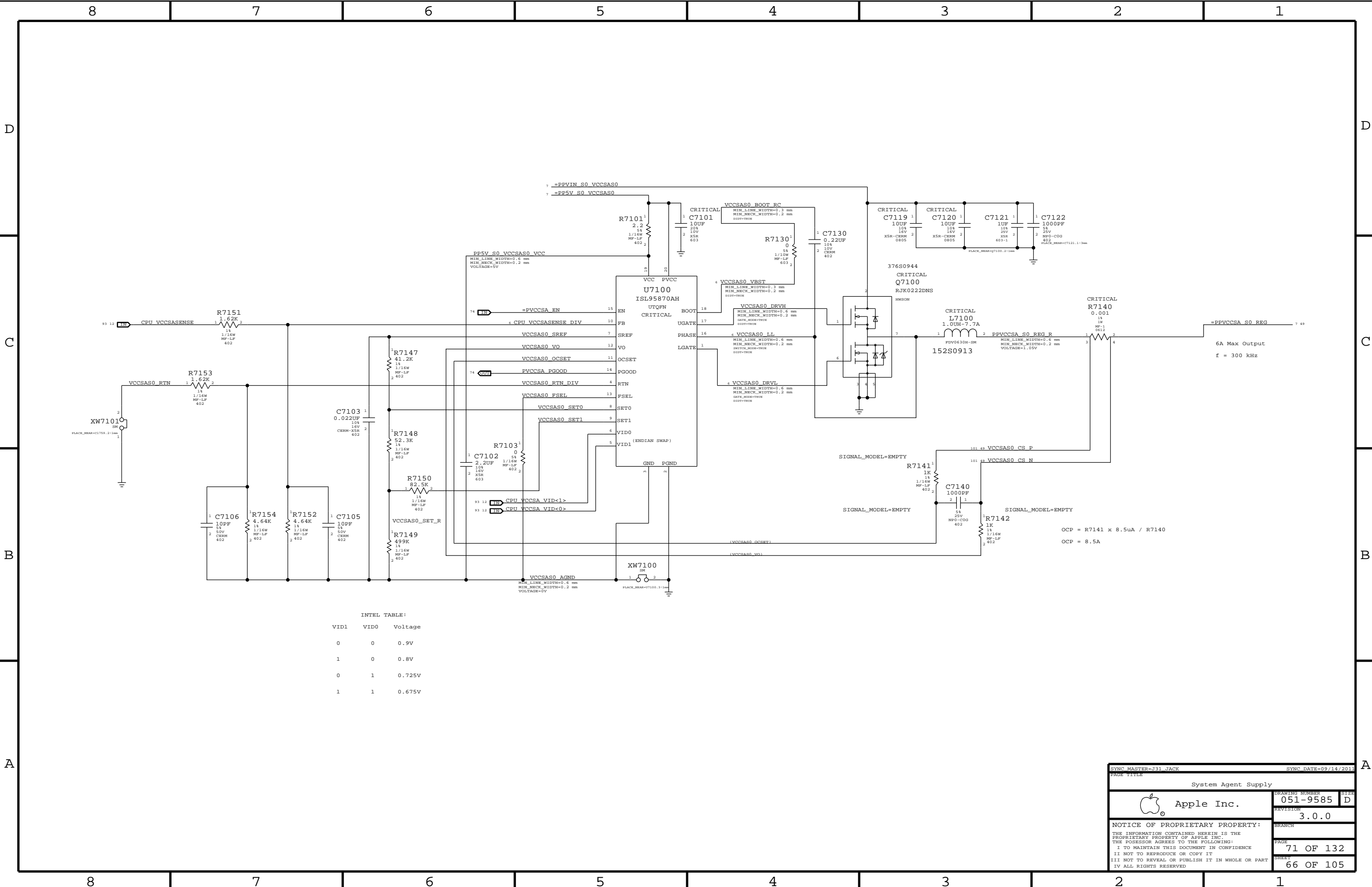
SYNC MASTER=J31 AUDIO		SYNC DATE=10/26/2011	
PAGE TITLE			
AUDIO: JACK TRANSLATORS			
 Apple Inc.		DRAWING NUMBER	051-9585
		SIZE	D
		REVISION	3.0.0
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		PAGE	68 OF 132
		SHEET	63 OF 105

MagSafe DC Power Jack

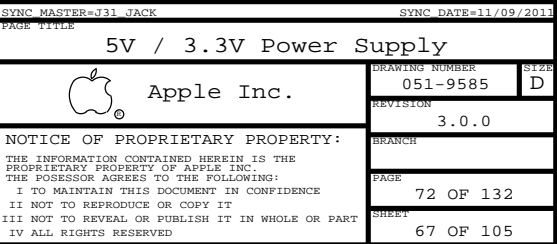


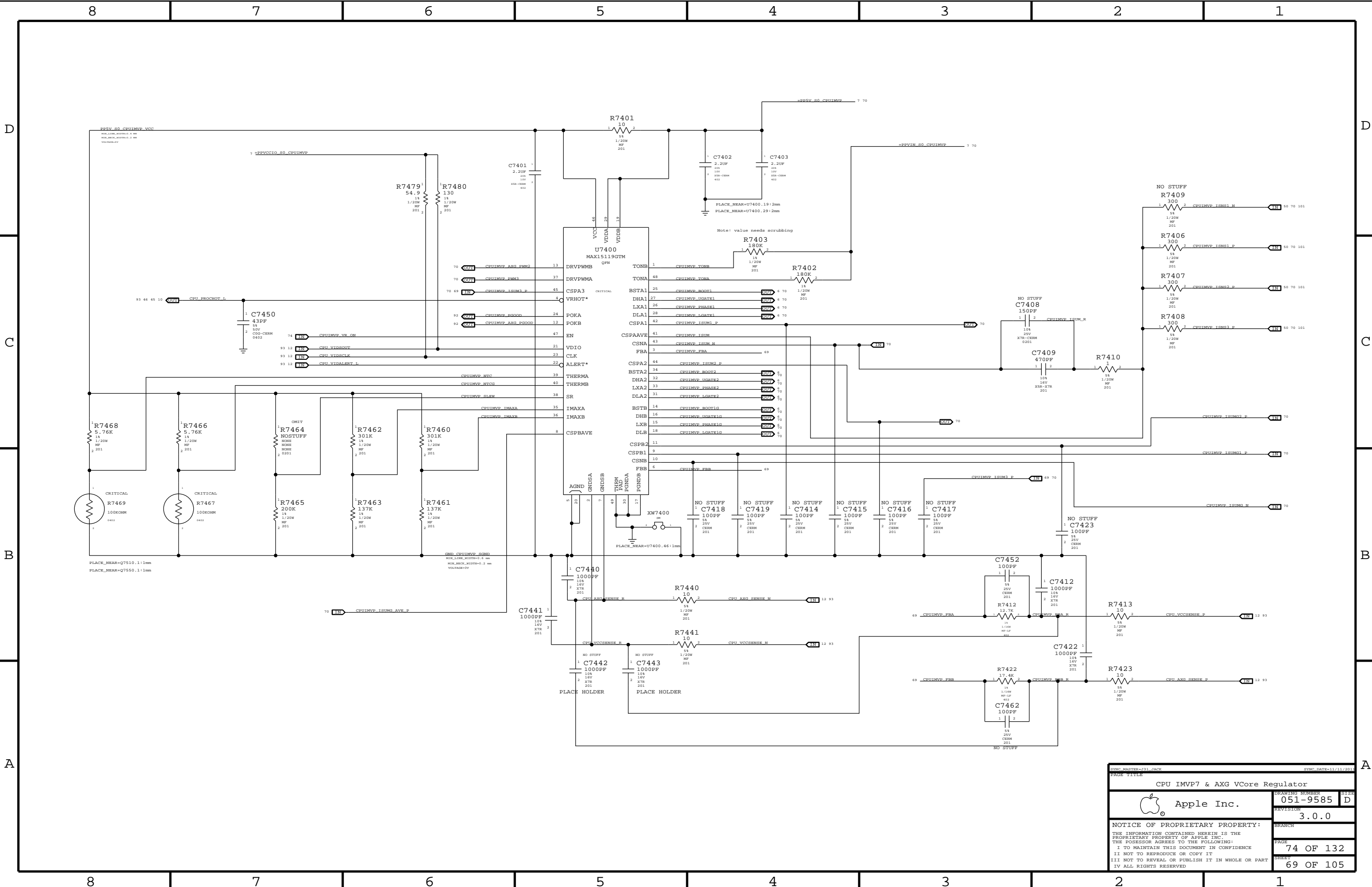
SYNC MASTER=J31 JACK		SYNC DATE=09/02/2011	
PAGE TITLE			
DC-In & Battery Connectors			
 Apple Inc.		DRAWING NUMBER	051-9585
		SHEET	D
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		BRANCH	
		PAGE	69 OF 132
		SHEET	64 OF 105

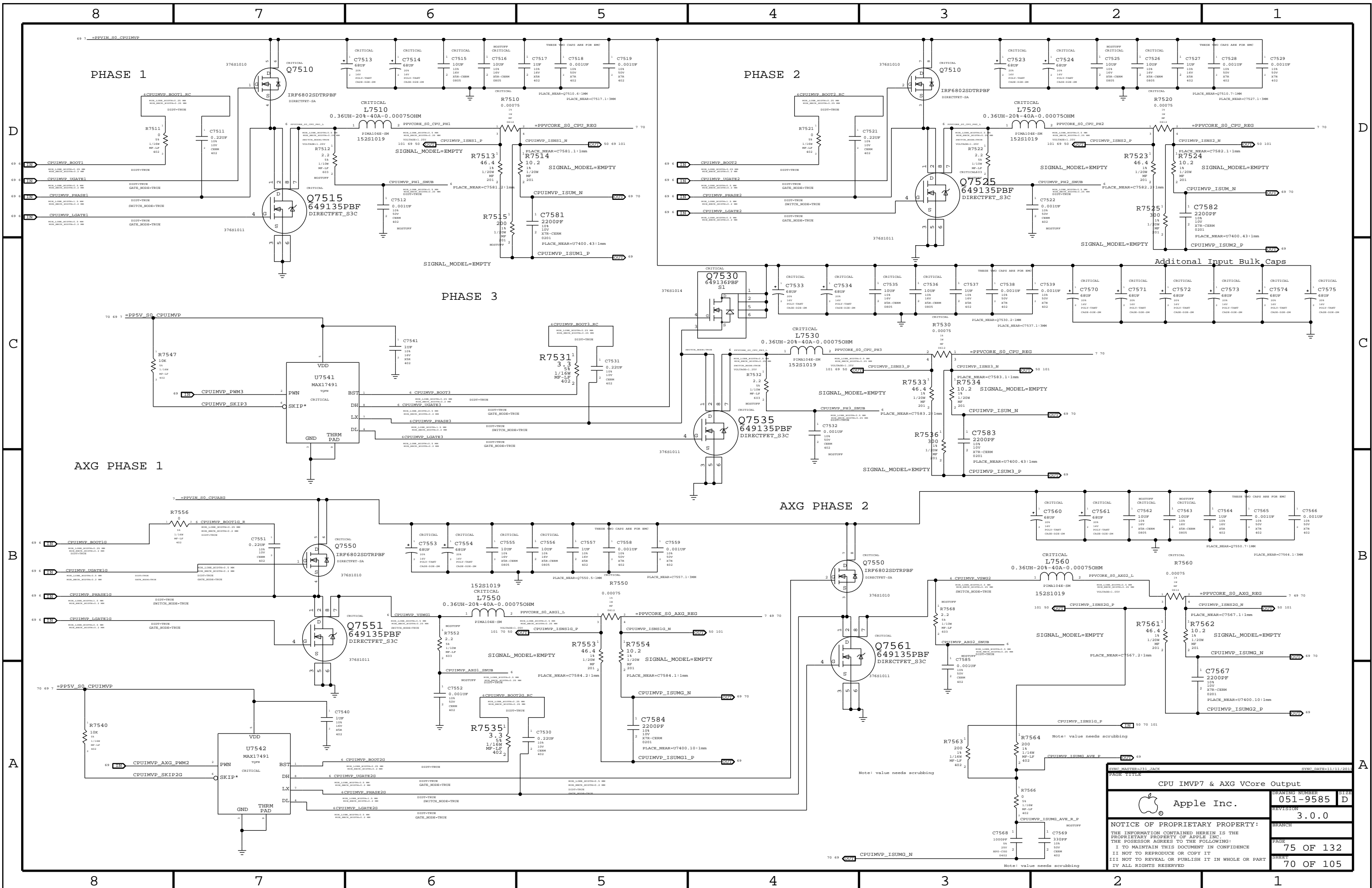




INTEL TABLE:		
VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V







SYSC PARTNERSHIP DATE

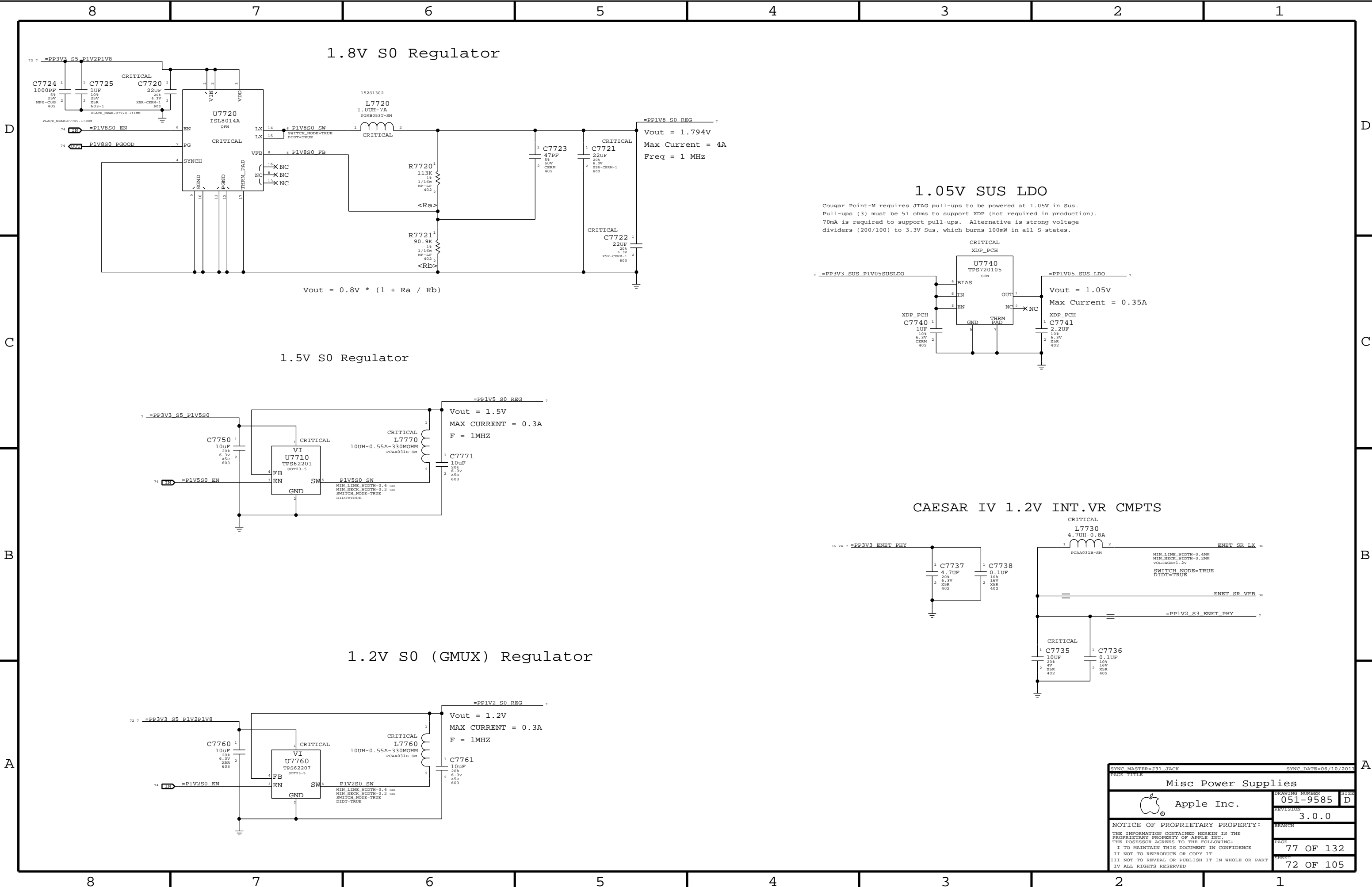
SYSC DATE: 11/11/2011

PAGE TITLE		SIZE
CPU IMPV7 & AXG VCore Output		D
Apple Inc.		051-9585
REVISION		3.0.0
BRANCH		
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1.8V S0 Regulator

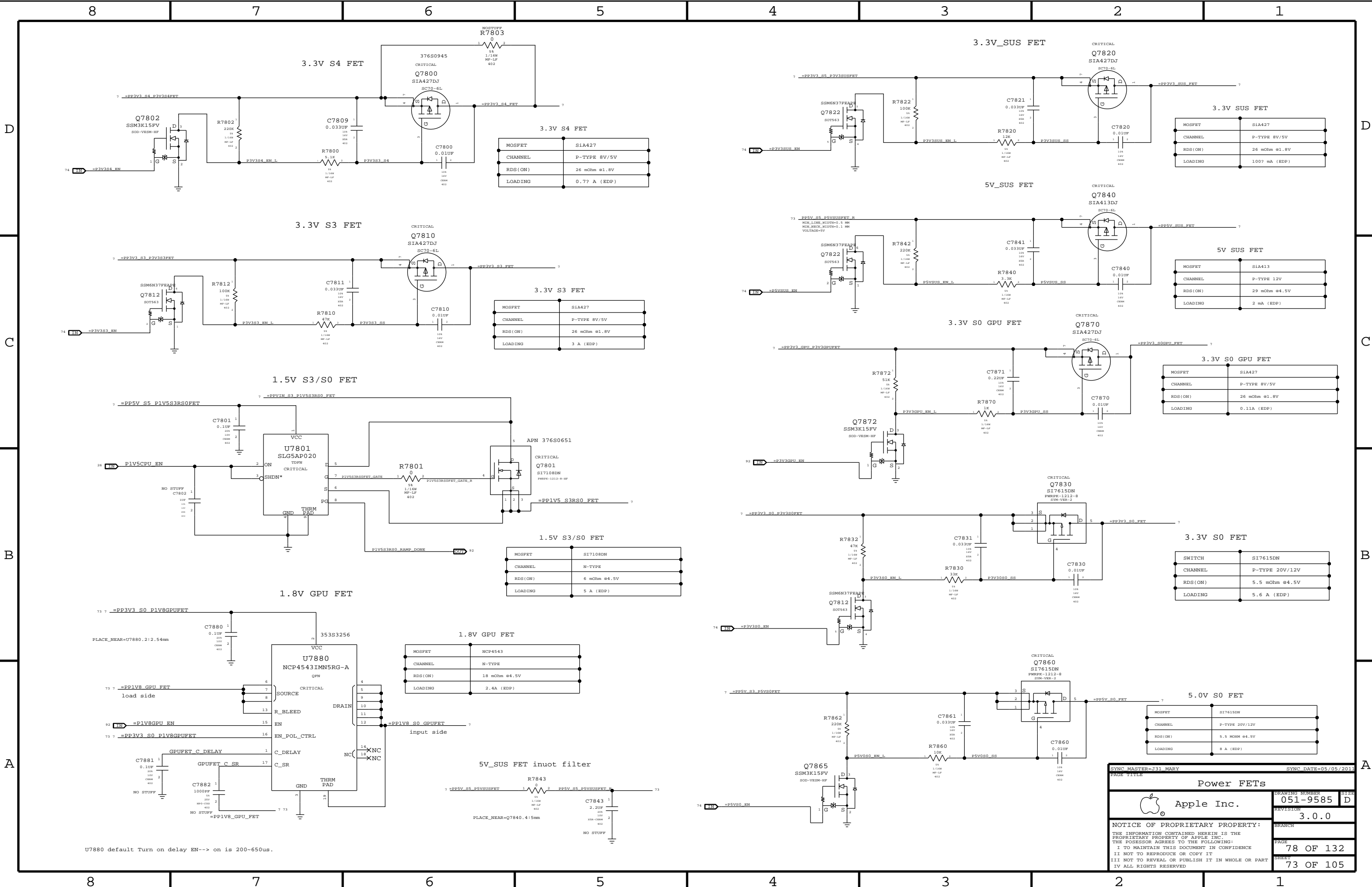
1.05V SUS LDO

1.5V S0 Regulator

1.2V S0 (GMUX) Regulator

CAESAR IV 1.2V INT.VR CMPTS

SYNC MASTER=J31 JACK		SYNC DATE=06/10/2013	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	051-9585
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SYNC MASTER=j31 MARY

SYNC DATE=05/05/2011

Power FETs

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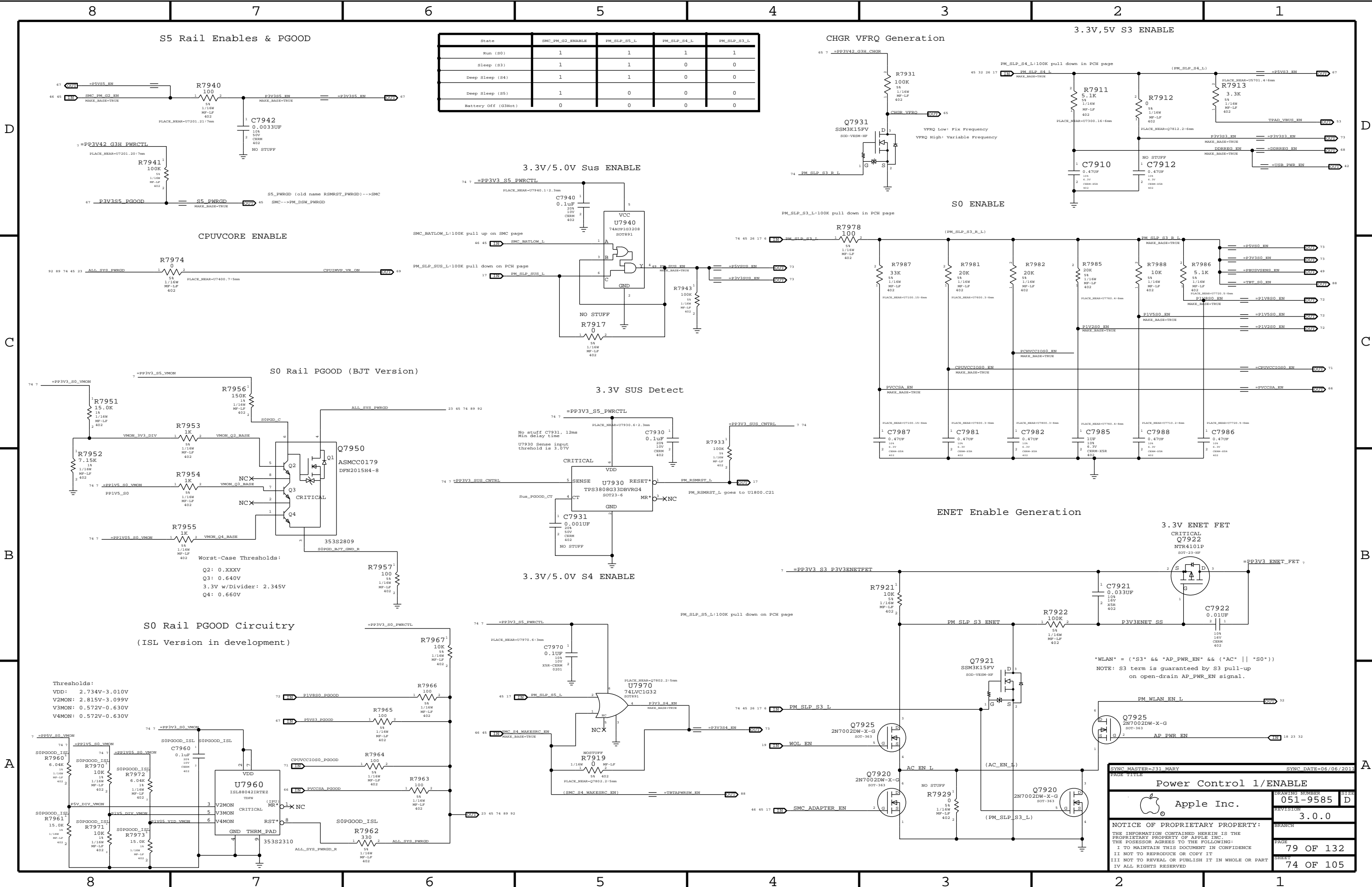
PAGE

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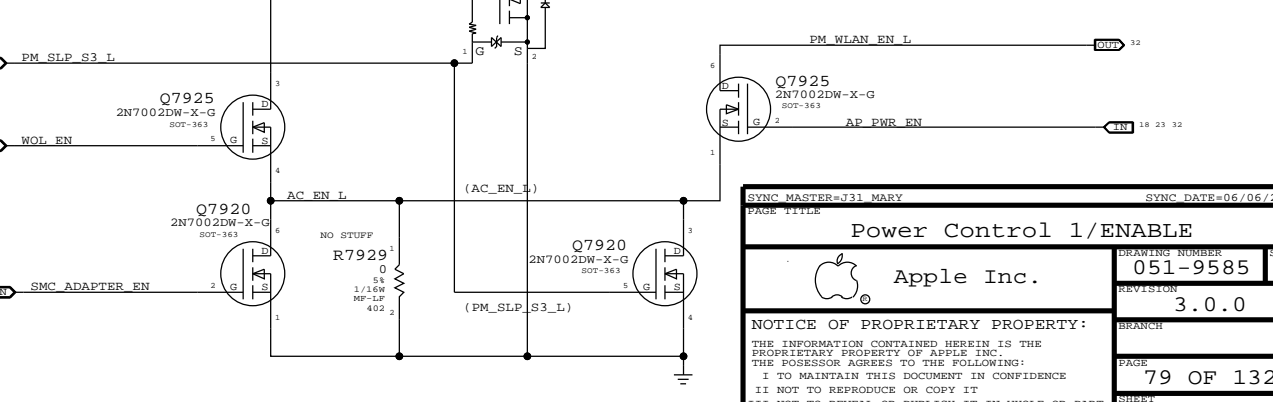
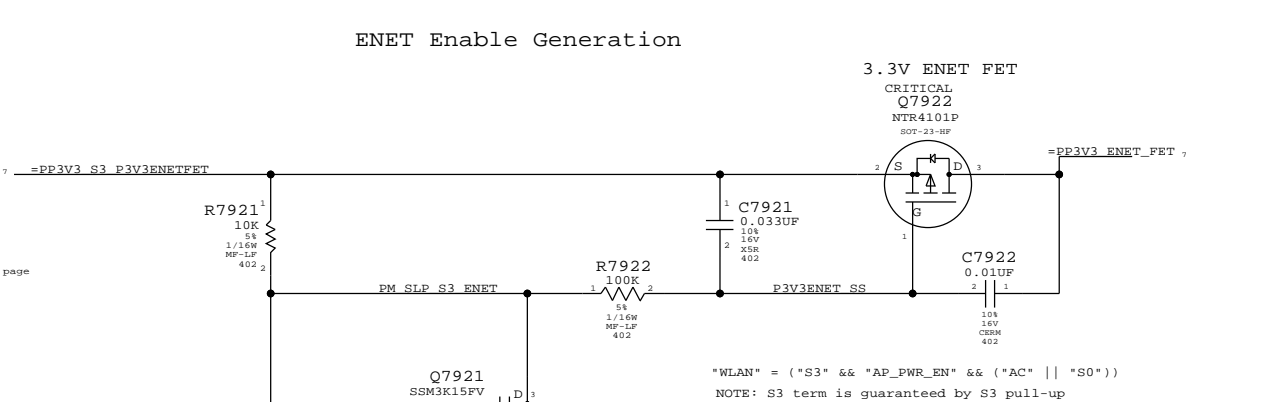
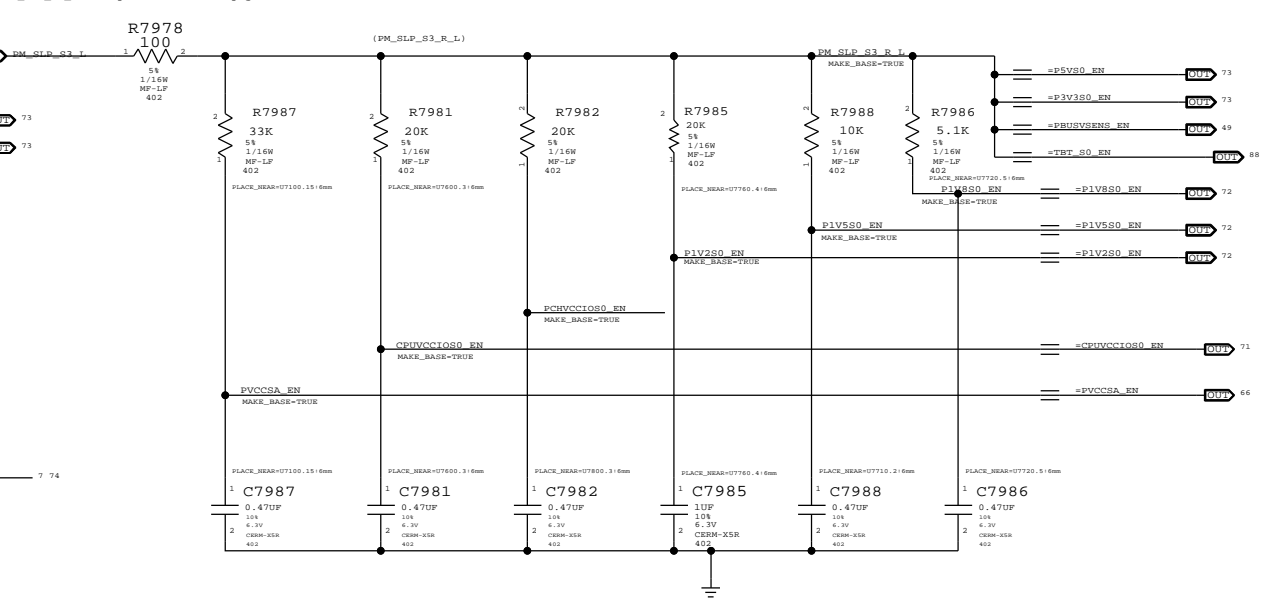
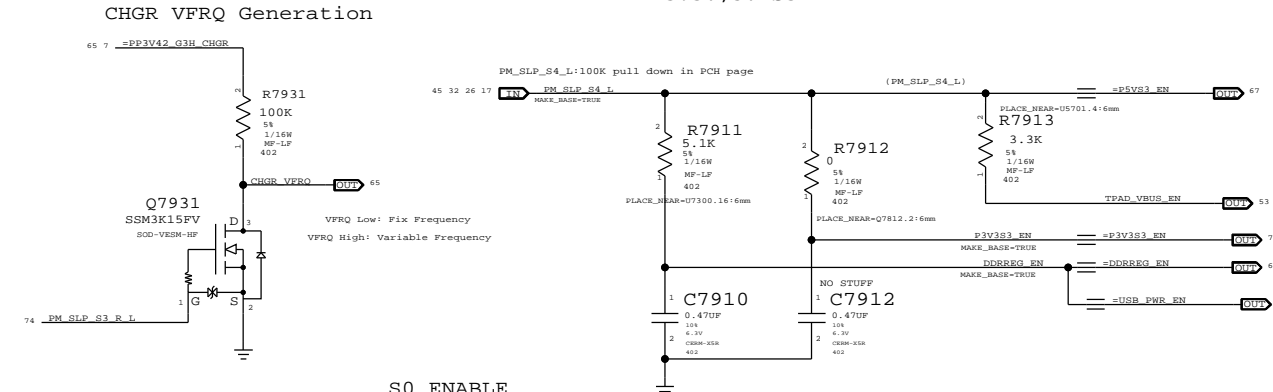
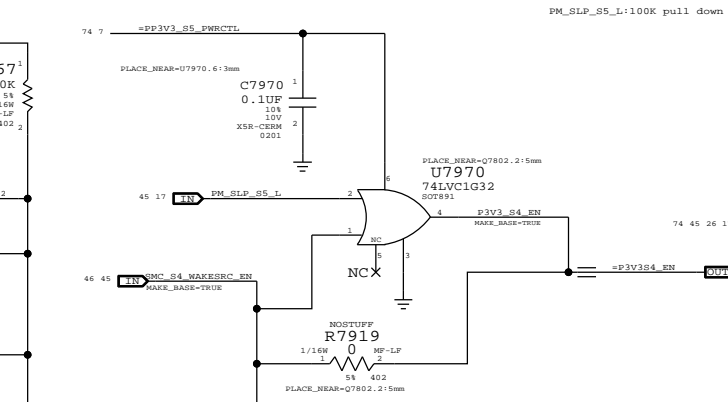
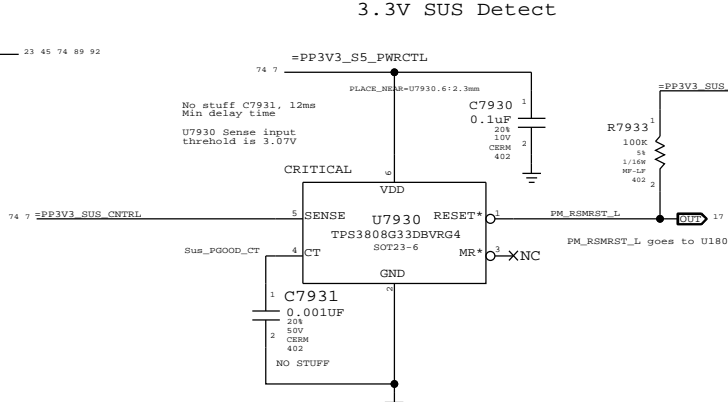
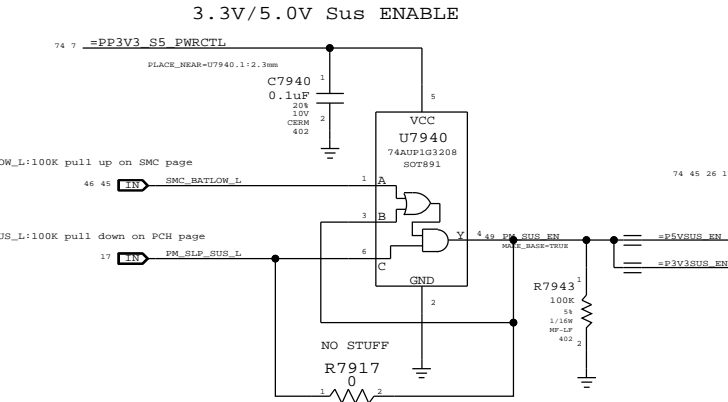
SHEET

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U7880 default Turn on delay EN--> on is 200-650us.



State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0



State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

A

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SYNC MASTER=J31 MARY

SYNC DATE=06/06/2013

Power Control 1/ENABLE

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Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33

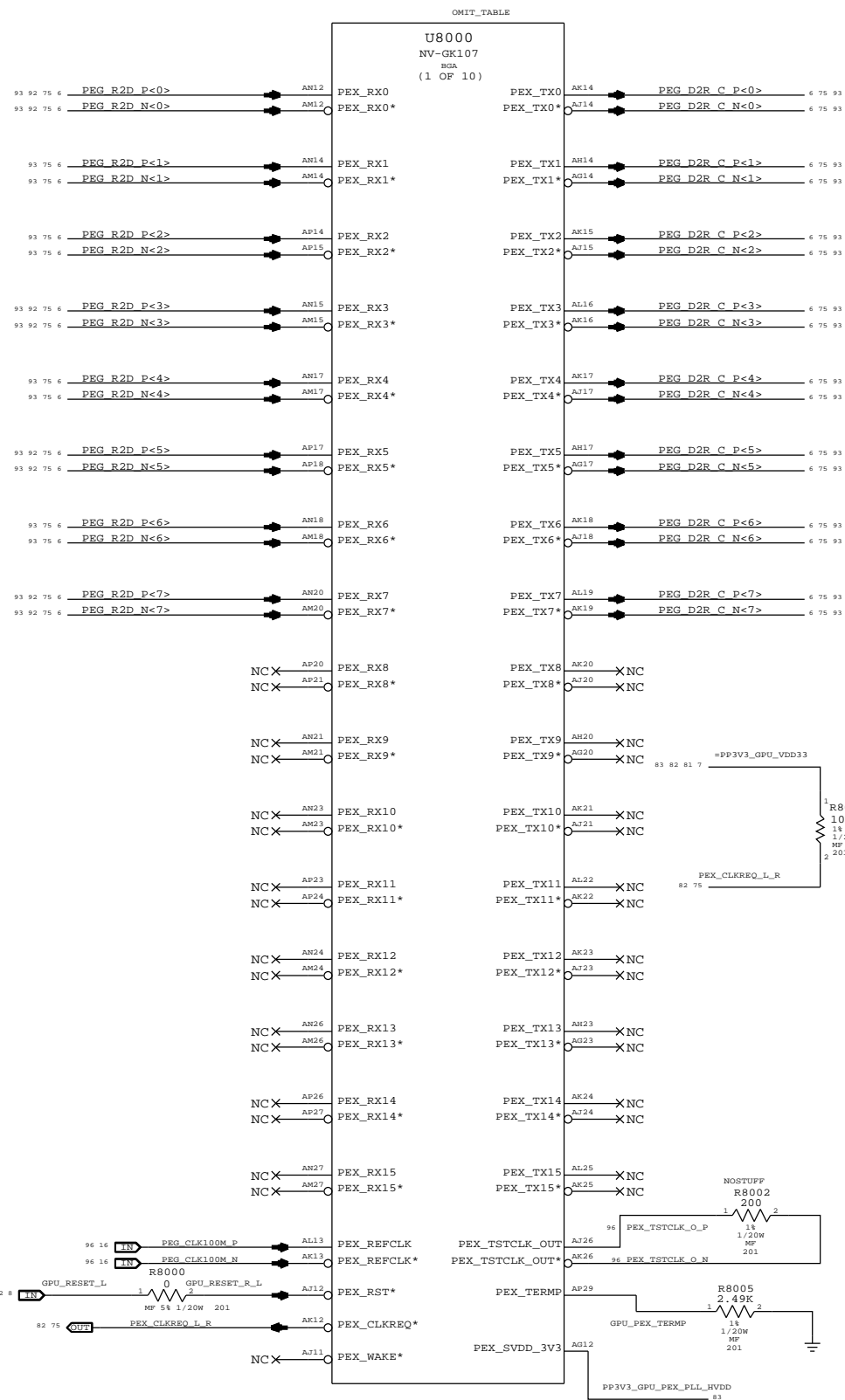
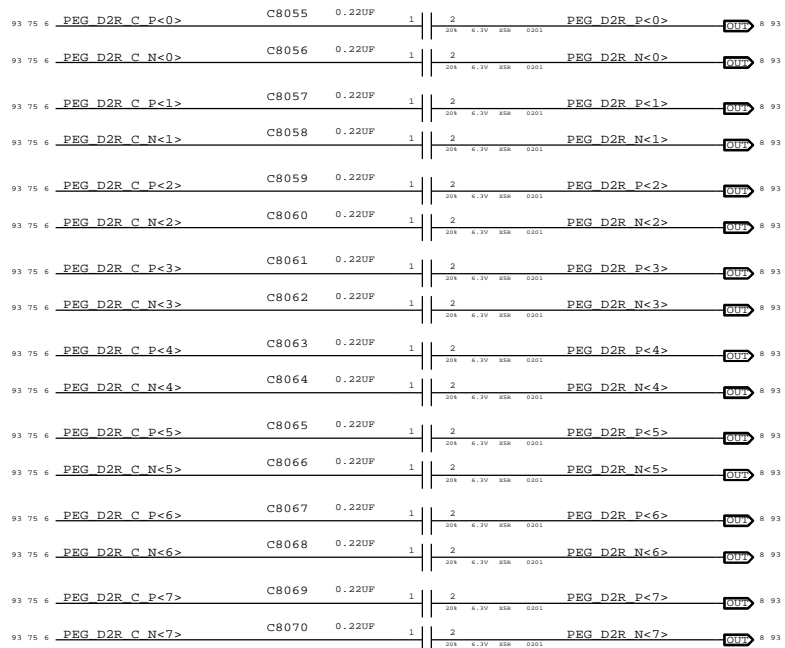
Signal aliases required by this page:
(NONE)


ECM options provided by this page

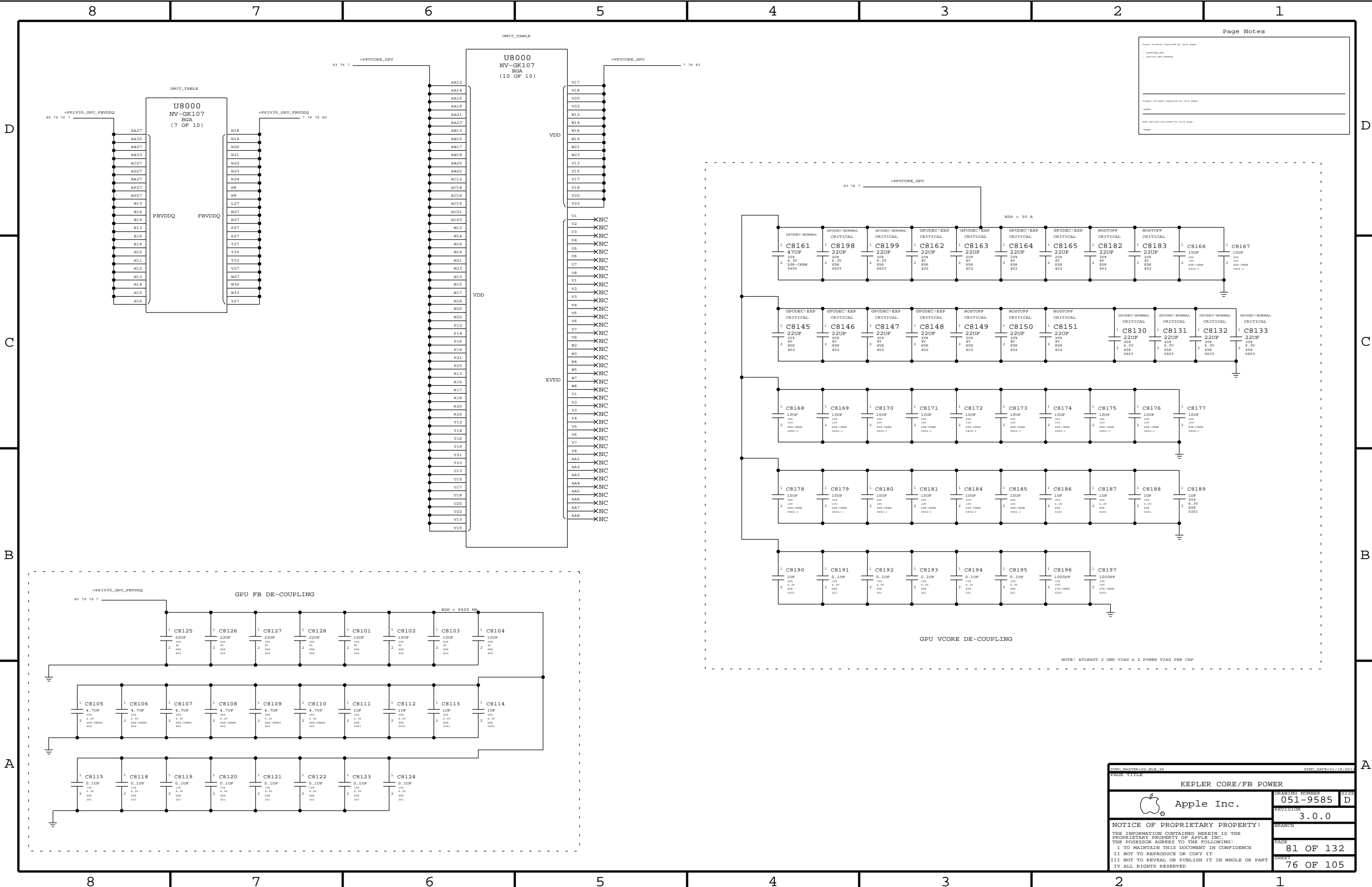
(NONE)




Note: Removed GND voids from AC caps for layout (J31).

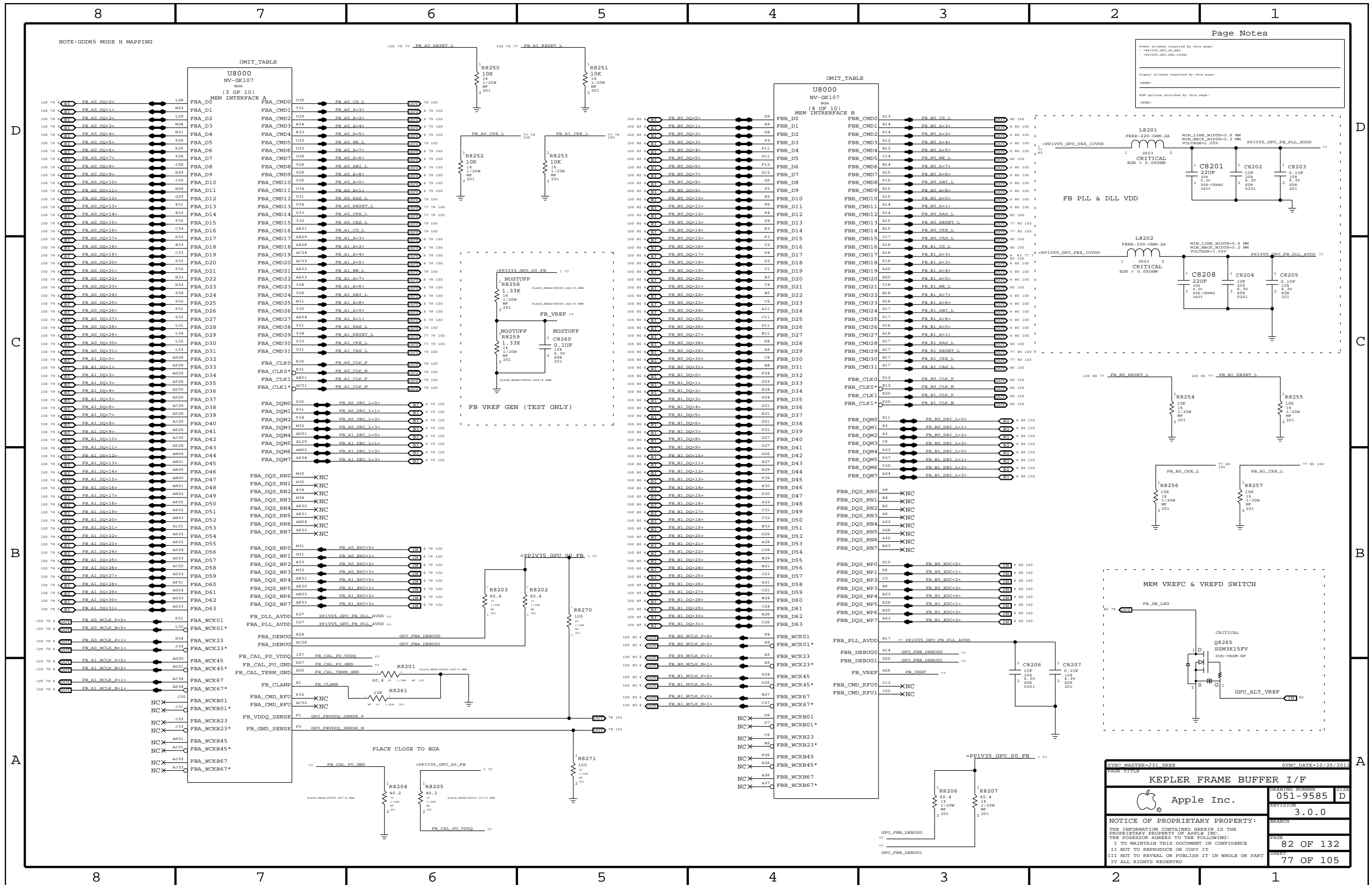


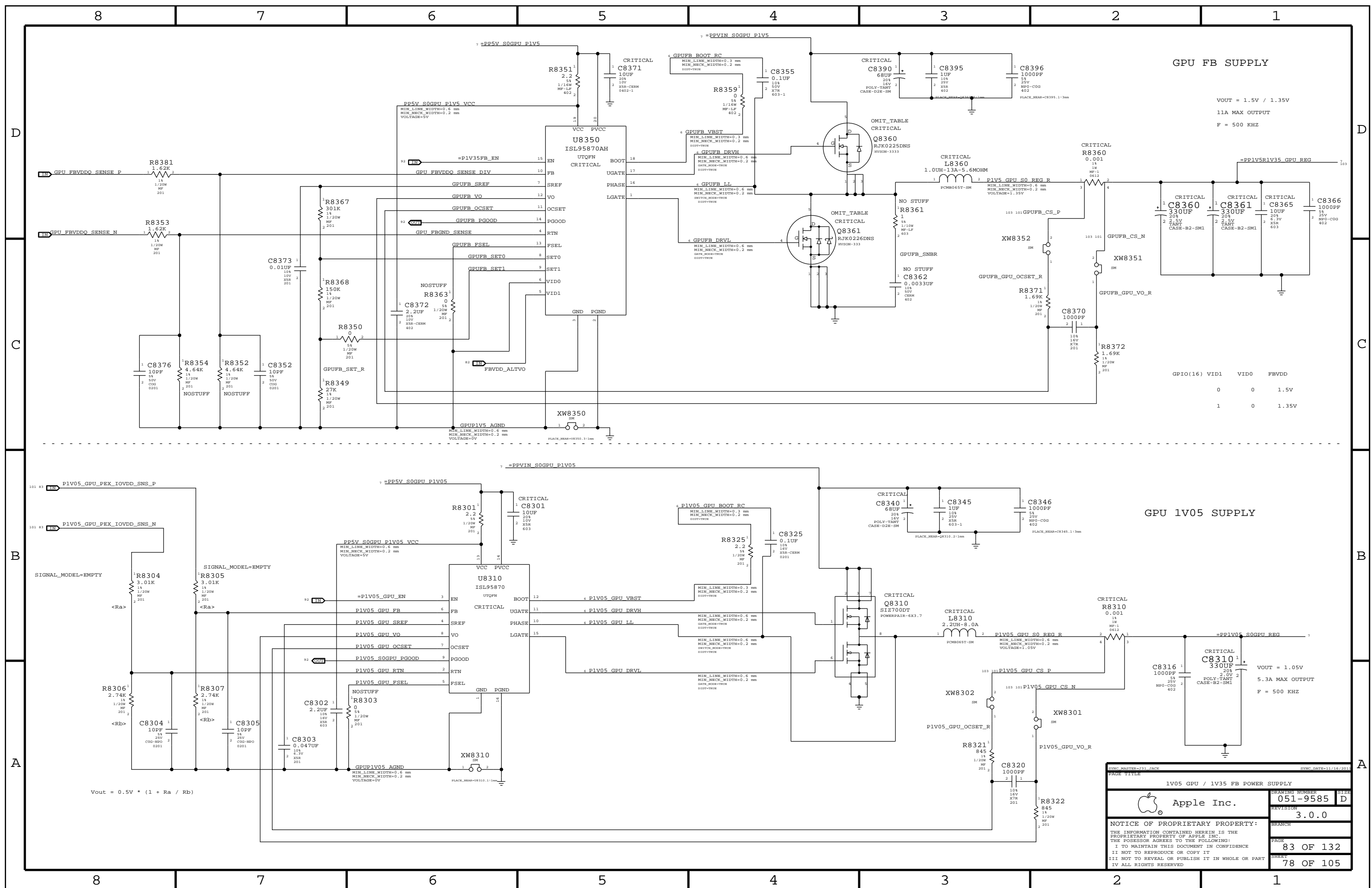
SYNCH MASTER=J31 SREE		SYNCH DATE=10/25/2011	
PAGE TITLE			
KEPLER PCI-E			
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		051-9585	
		SIZE	
		D	
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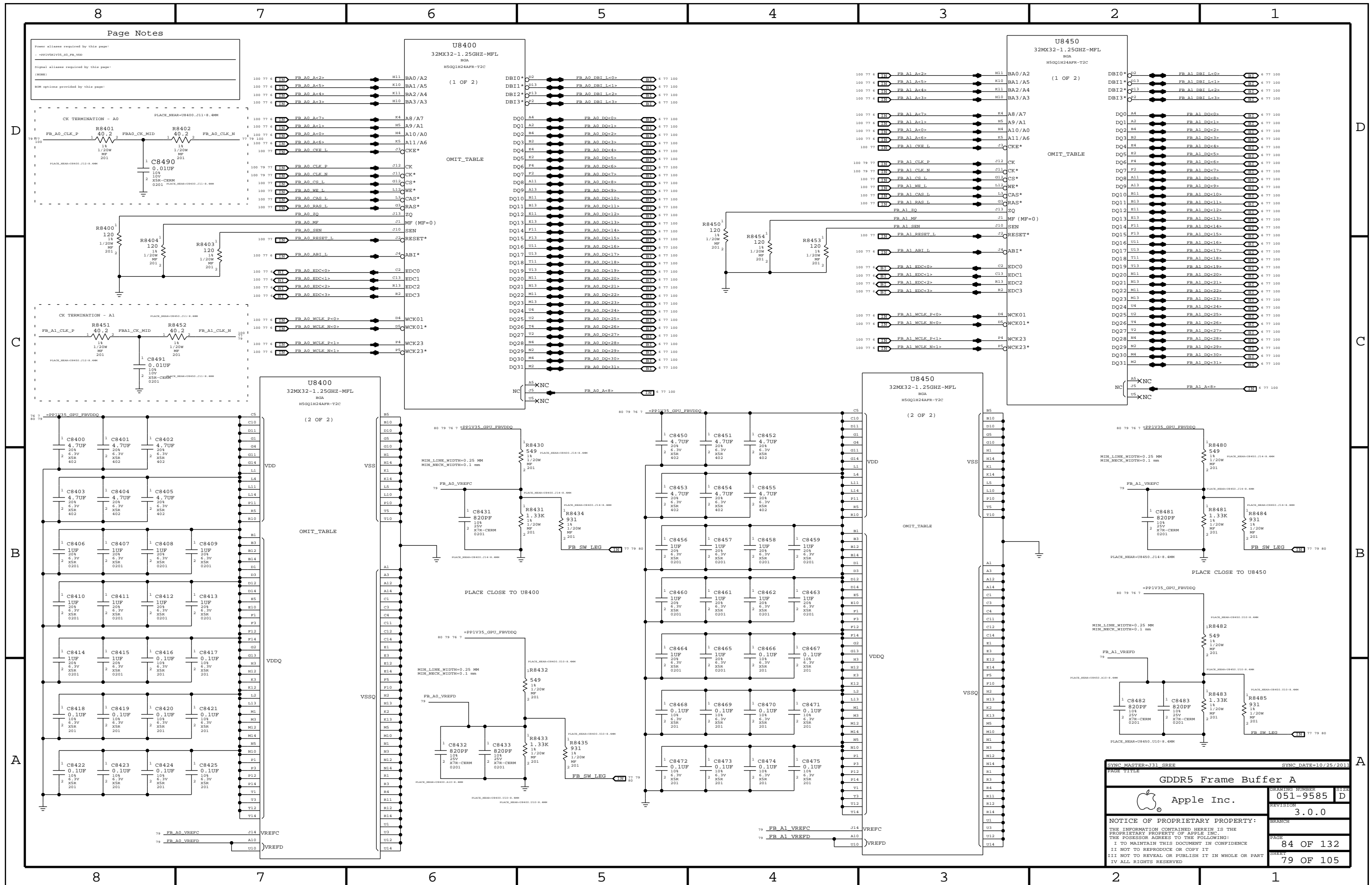


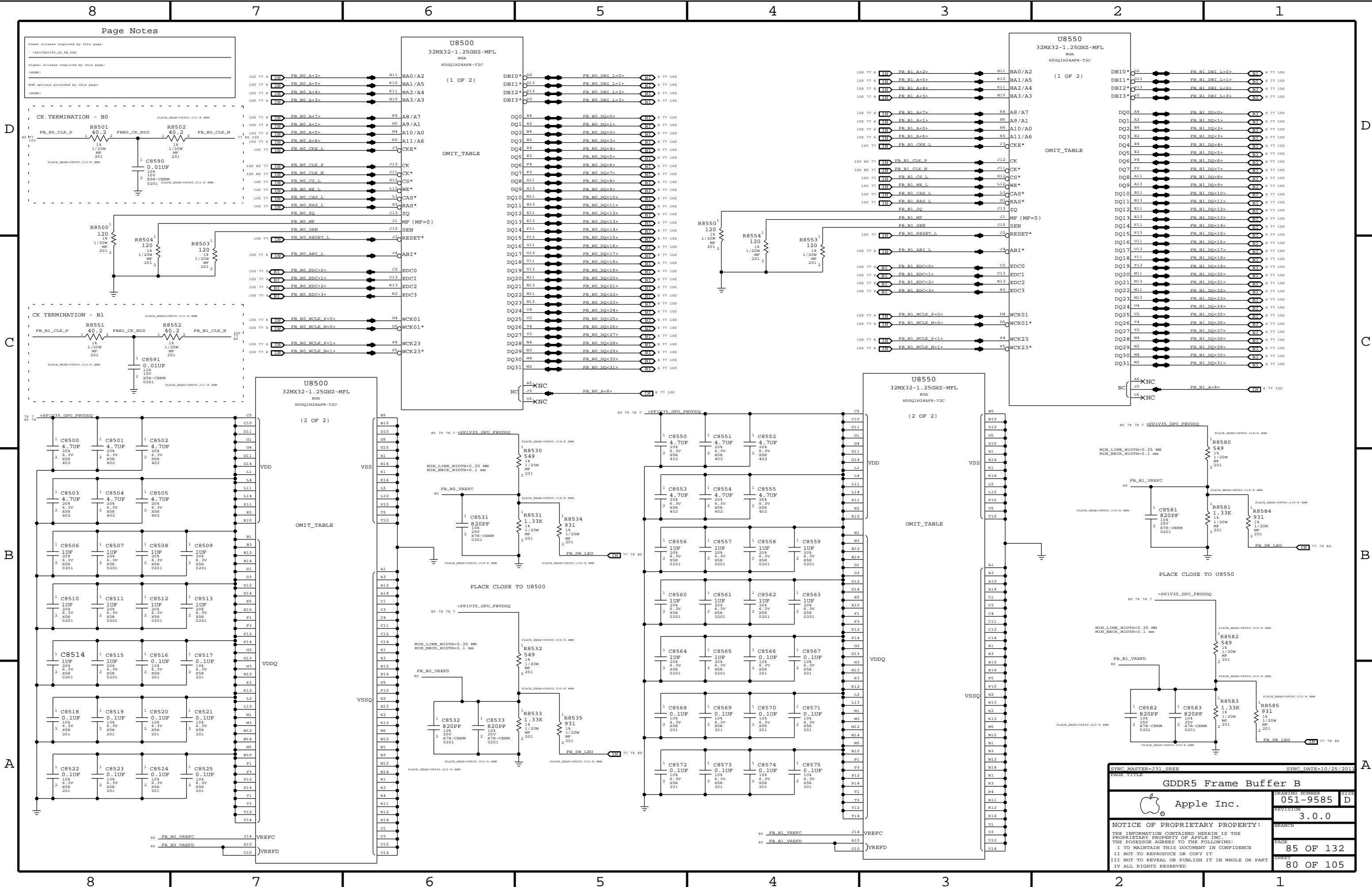
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Power aliases required by this page:	
- vppcore_gm	
- vppcore_gm_pwrng	
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

SYNCHARTER-001_M01_02		SYNCHARTER-001_M01_02	
PAGE TITLE			
KEPLER CORE/FB POWER			
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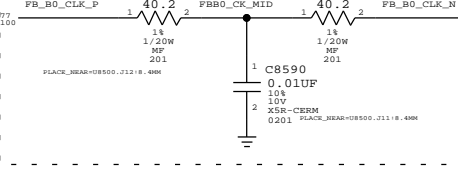
Page Notes

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- ~PP1V35_GPU_FBVDDQ

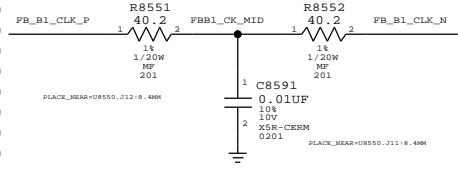
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SNM options provided by this page:
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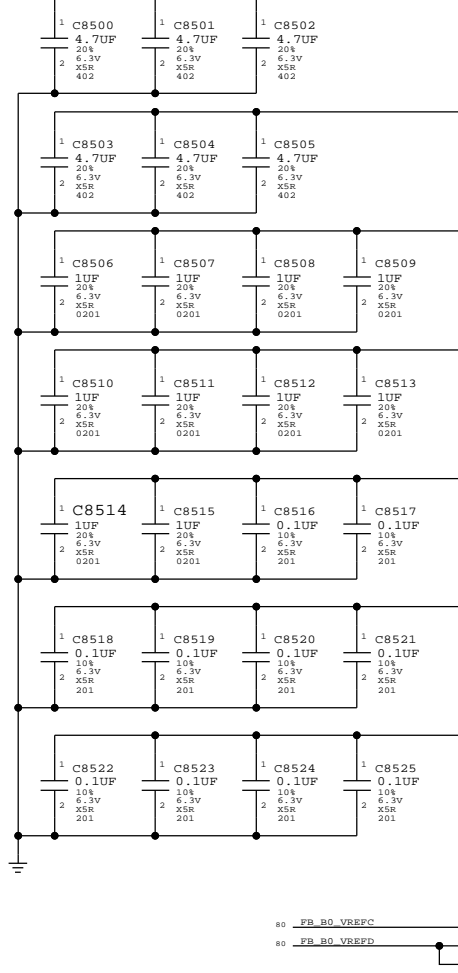
CK TERMINATION - B0



CK TERMINATION - B1



POWER



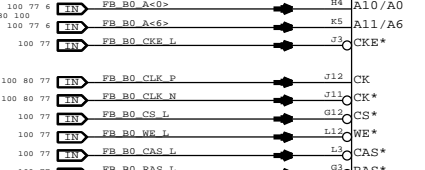
U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

DBI0*
DBI1*
DBI2*
DBI3*

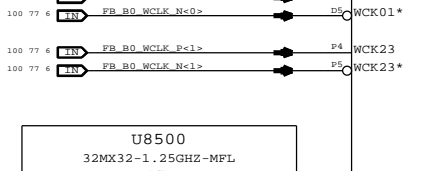
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*

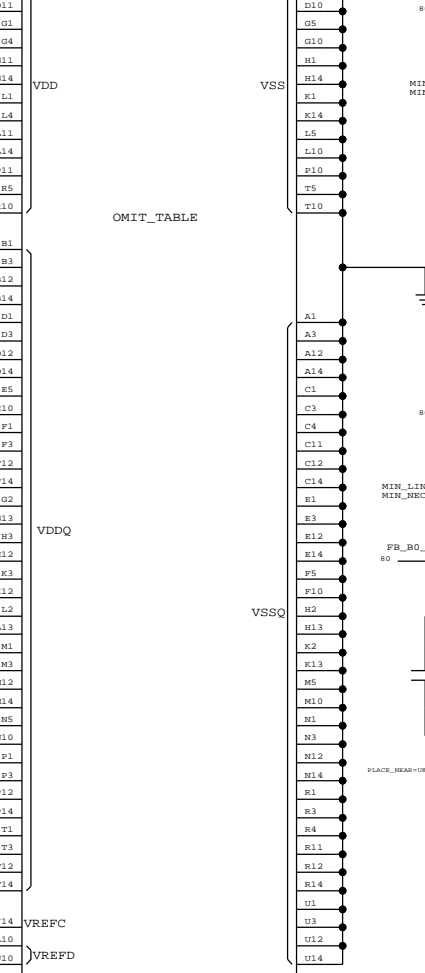
CK TERMINATION - B0



CK TERMINATION - B1



POWER



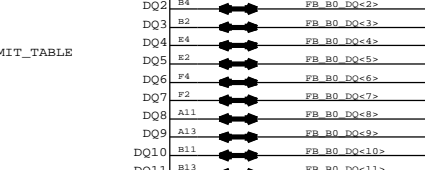
U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

DBI0*
DBI1*
DBI2*
DBI3*

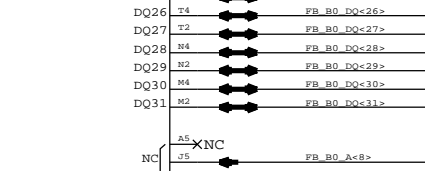
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*

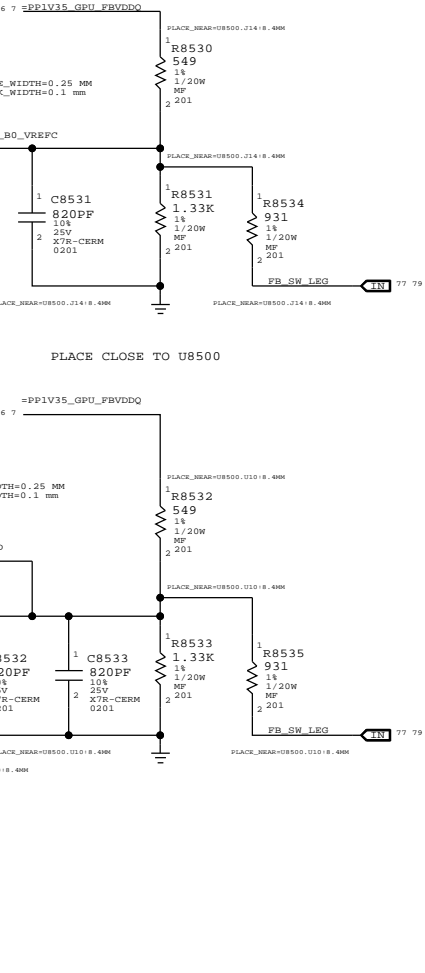
CK TERMINATION - B0



CK TERMINATION - B1



POWER



U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

DBI0*
DBI1*
DBI2*
DBI3*

DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
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DQ7
DQ8
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DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*

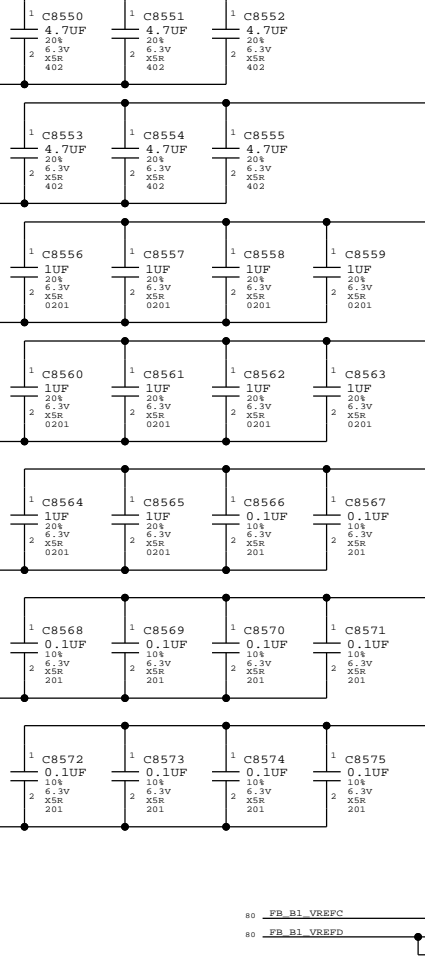
CK TERMINATION - B0



CK TERMINATION - B1



POWER



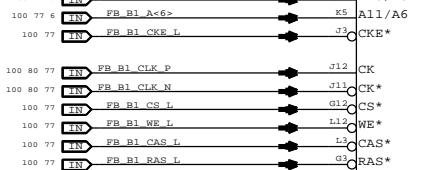
U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

DBI0*
DBI1*
DBI2*
DBI3*

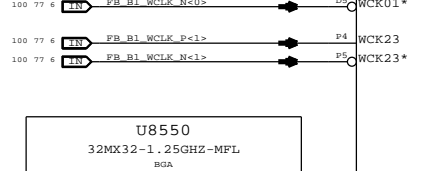
DQ0
DQ1
DQ2
DQ3
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DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
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DQ30
DQ31

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*

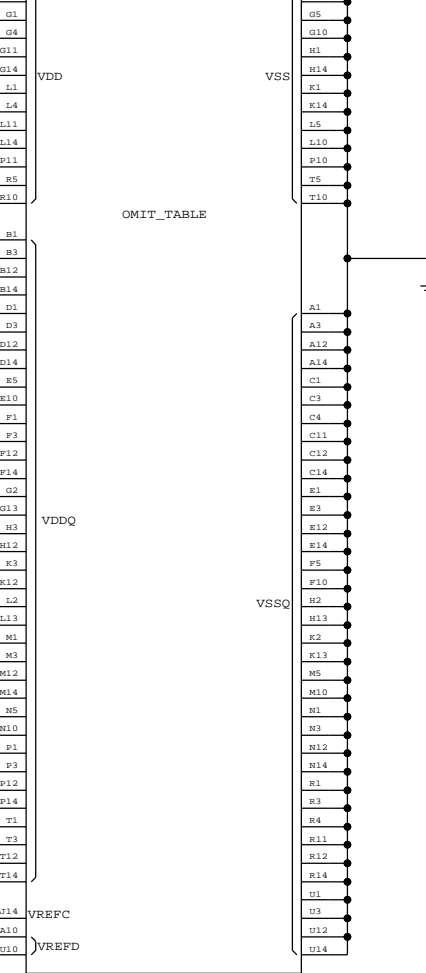
CK TERMINATION - B0



CK TERMINATION - B1



POWER



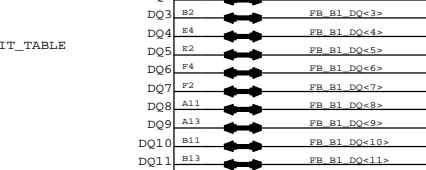
U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

DBI0*
DBI1*
DBI2*
DBI3*

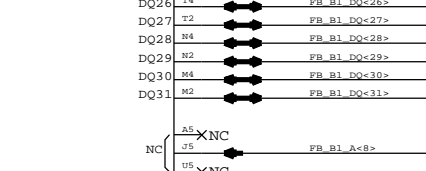
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DQ29
DQ30
DQ31

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*

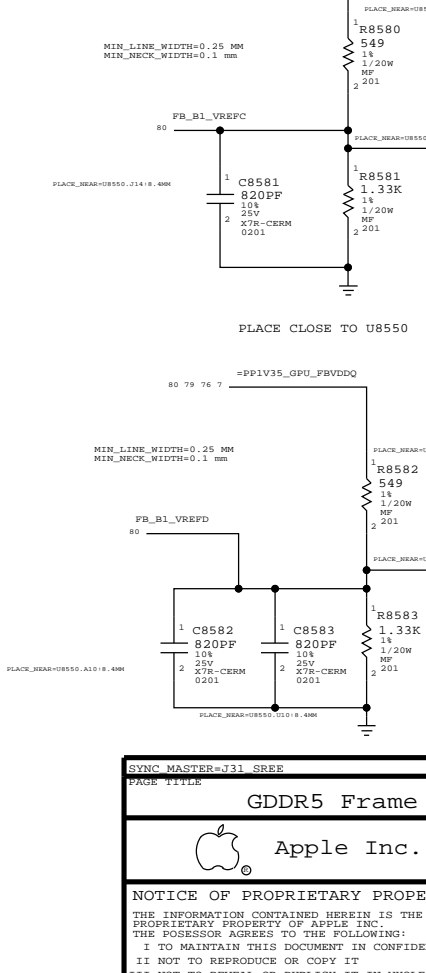
CK TERMINATION - B0



CK TERMINATION - B1



POWER



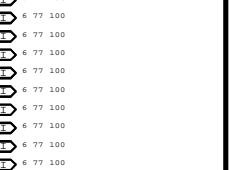
U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

DBI0*
DBI1*
DBI2*
DBI3*

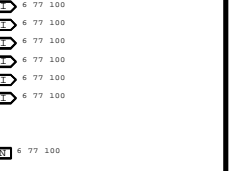
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DQ1
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DQ29
DQ30
DQ31

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*

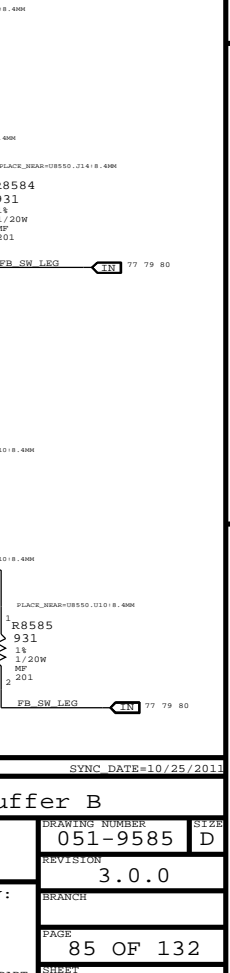
CK TERMINATION - B0

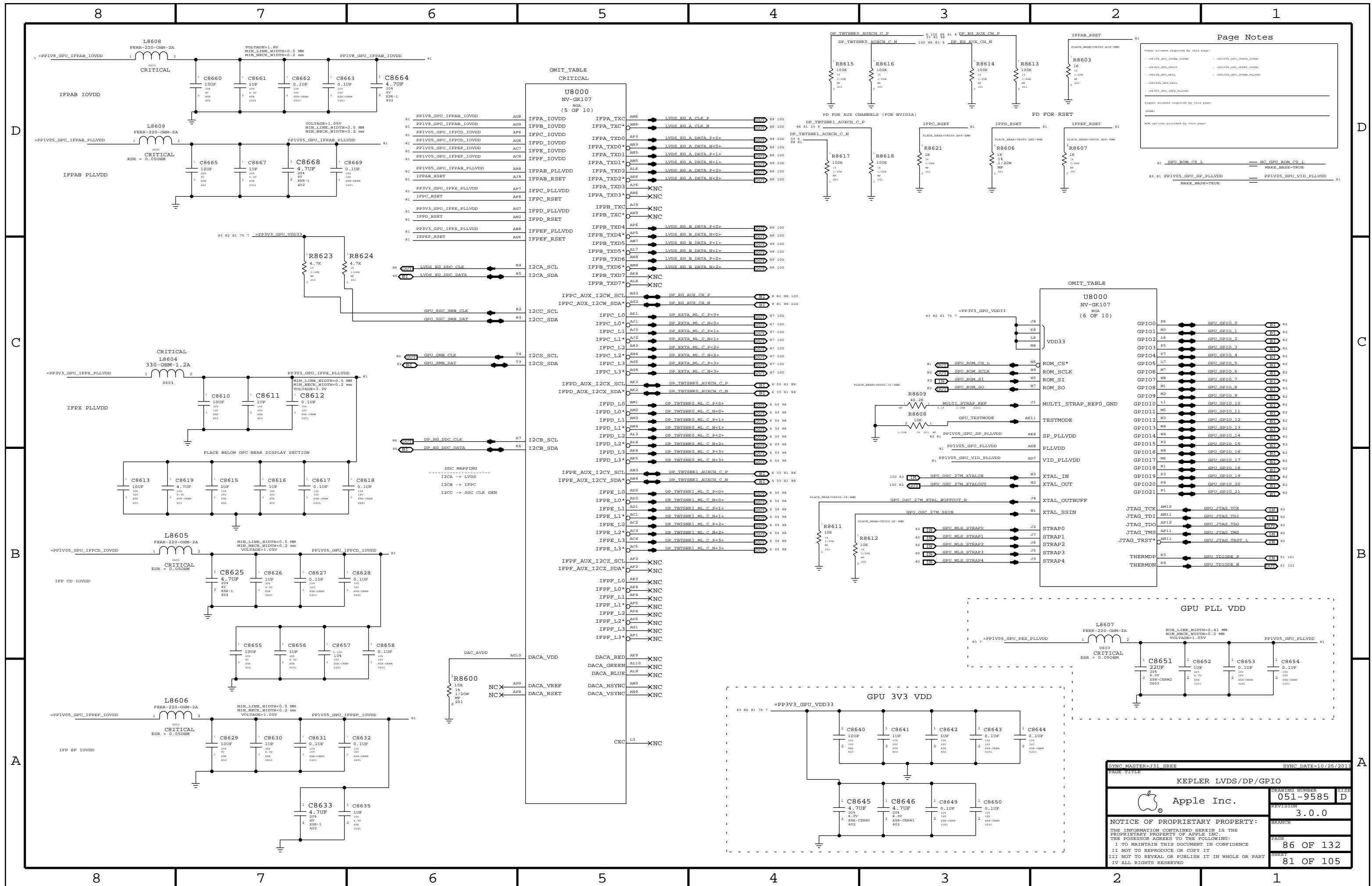


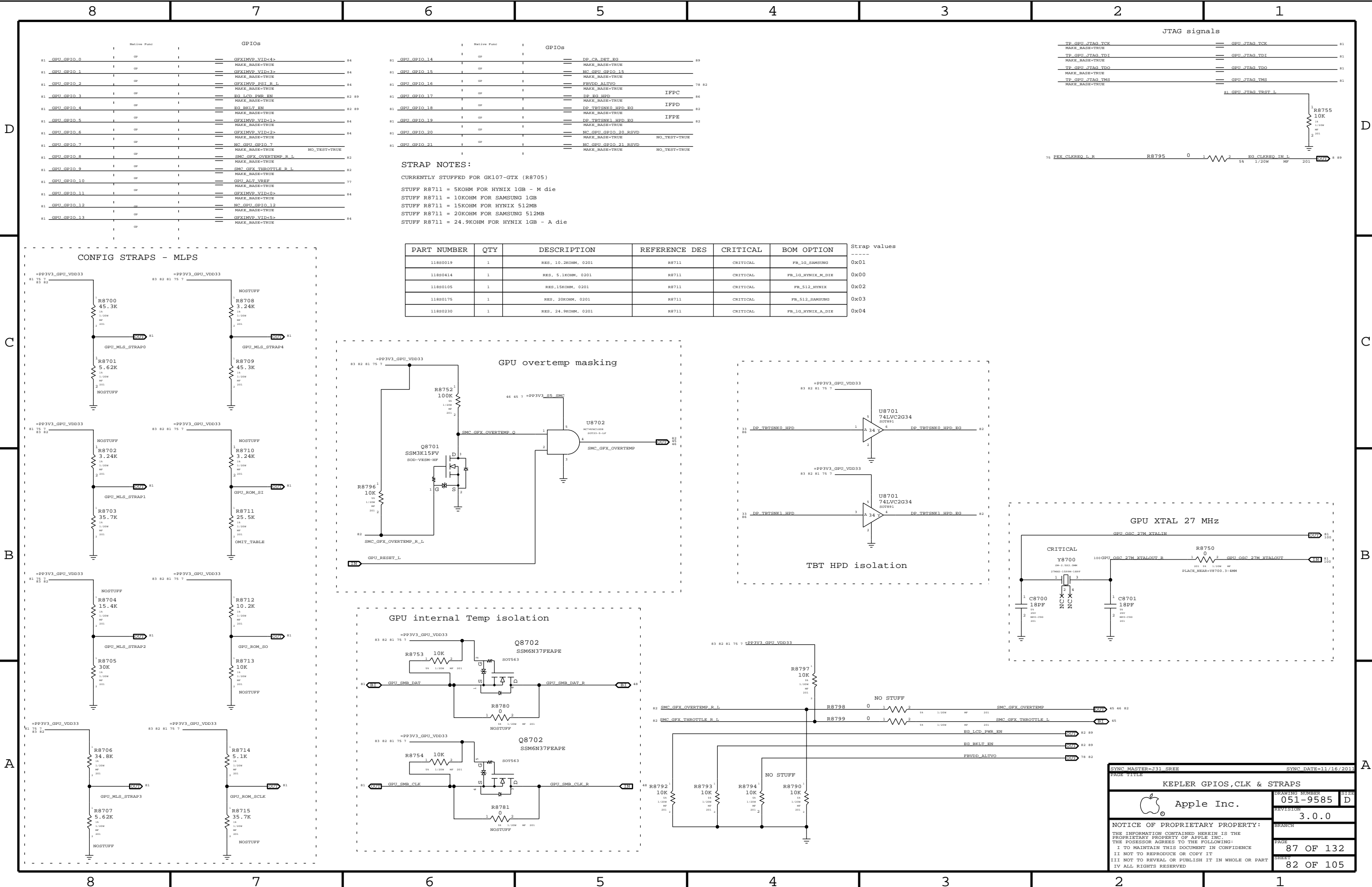
CK TERMINATION - B1



POWER







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STRAP NOTES:
CURRENTLY STUFFED FOR GK107-GTX (R8705)
STUFF R8711 = 5KOHM FOR HYNIX 1GB - M die
STUFF R8711 = 10KOHM FOR SAMSUNG 1GB
STUFF R8711 = 15KOHM FOR HYNIX 512MB
STUFF R8711 = 20KOHM FOR SAMSUNG 512MB
STUFF R8711 = 24.9KOHM FOR HYNIX 1GB - A die

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880019	1	RES, 10.2KOHM, 0201	R8711	CRITICAL	FB_1G_SAMSUNG
11880414	1	RES, 5.1KOHM, 0201	R8711	CRITICAL	FB_1G_HYNIX_M_DIE
11880105	1	RES, 15KOHM, 0201	R8711	CRITICAL	FB_512_HYNIX
11880175	1	RES, 20KOHM, 0201	R8711	CRITICAL	FB_512_SAMSUNG
11880230	1	RES, 24.9KOHM, 0201	R8711	CRITICAL	FB_1G_HYNIX_A_DIE

Strap values

0x01
0x00
0x02
0x03
0x04

SYNC MASTER=j31 SREE

SYNC DATE=11/16/2011

KEPLER GPIOs,CLK & STRAPS

Apple Inc.

DRAWING NUMBER
051-9585

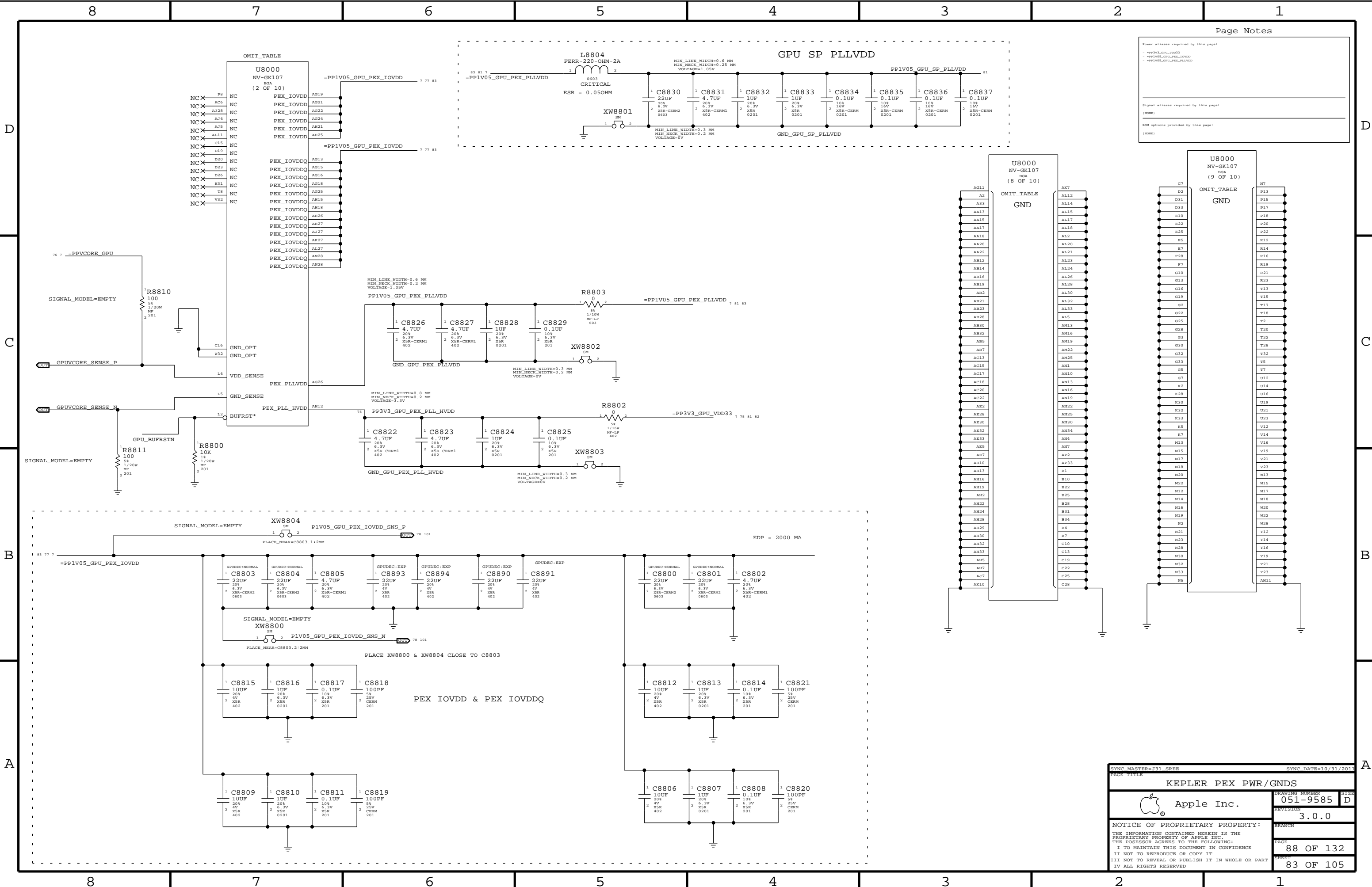
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Page Notes

Power aliases required by this page:

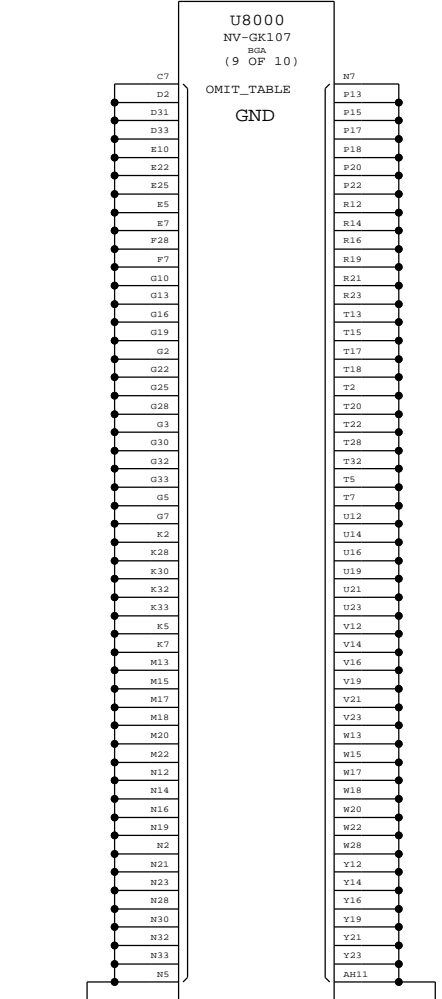
- PP3V3_GPU_VDD33
- PP1V05_GPU_PEX_IOVDD
- PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

NOT options provided by this page:

(NONE)



SYNC MASTER=J31 SREE

SYNC DATE=10/31/2011

DRAWING NUMBER

051-9585

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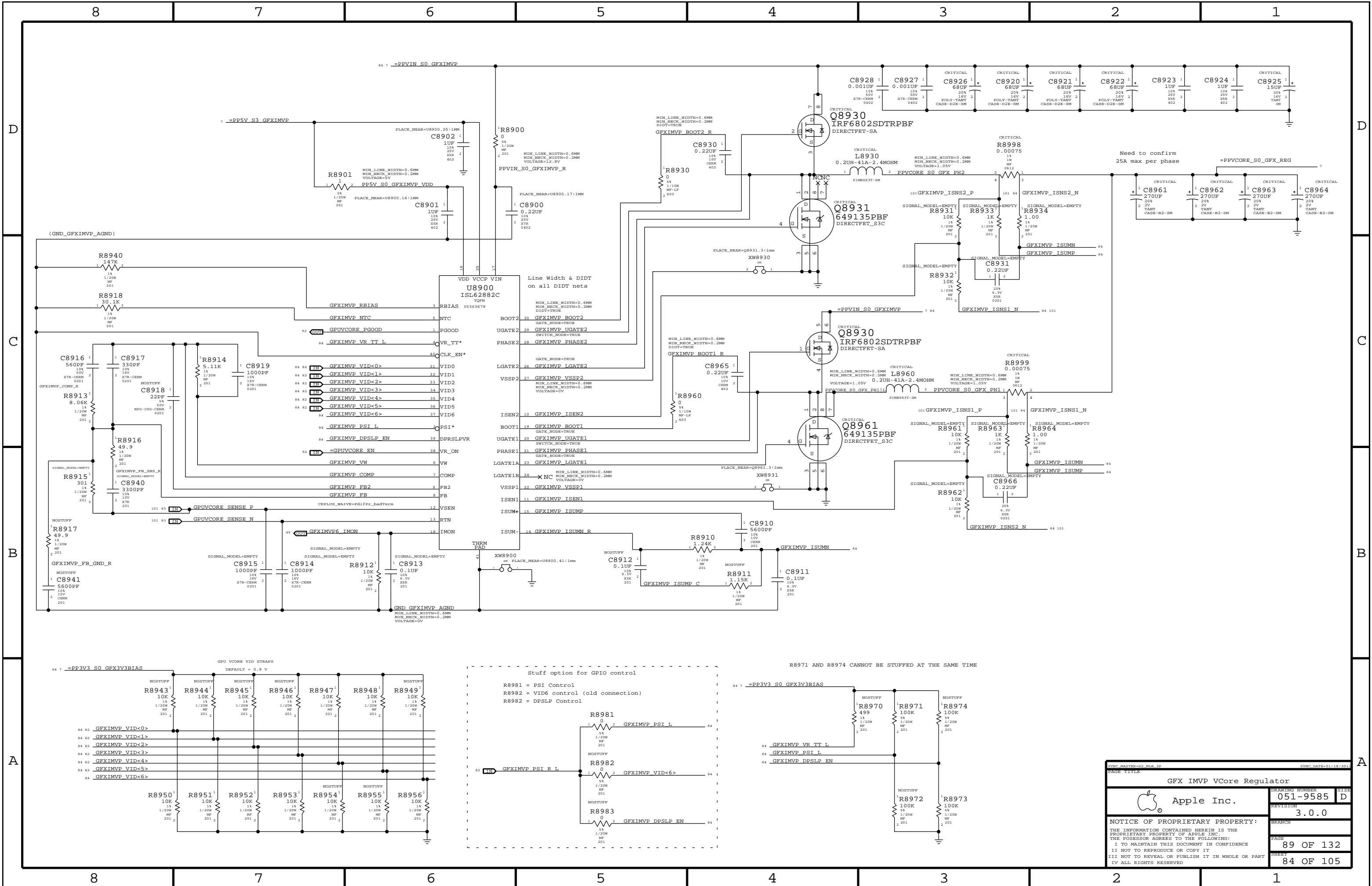
SHEET

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KEPLER PEX PWR/GNDS

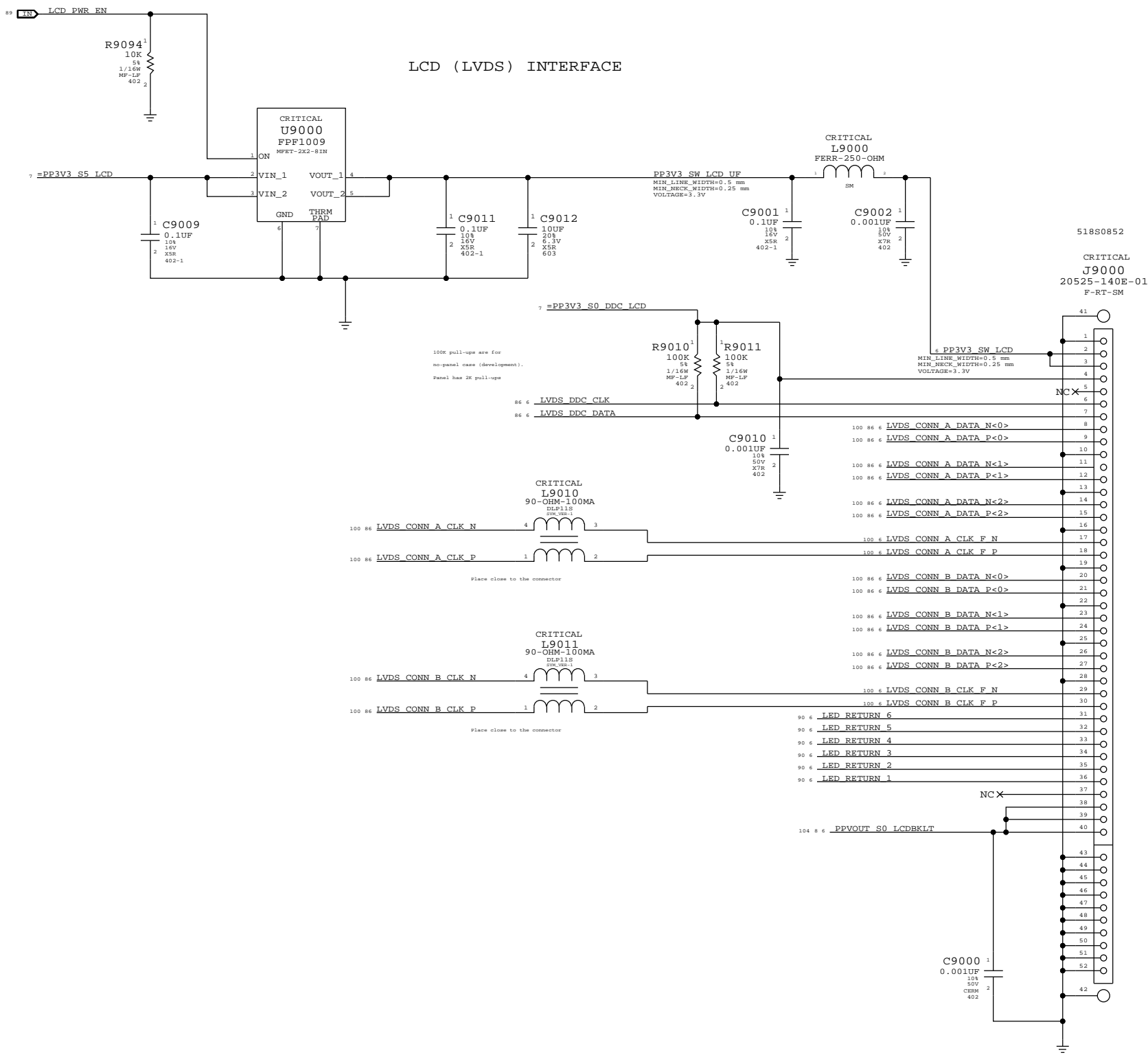
Apple Inc.


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SYNC MASTER=K18 MLB		SYNC DATE=04/27/2010	
PAGE TITLE			
LVDS Display Connector			
 Apple Inc.	DRAWING NUMBER		D
	051-9585		
	REVISION		
		3.0.0	
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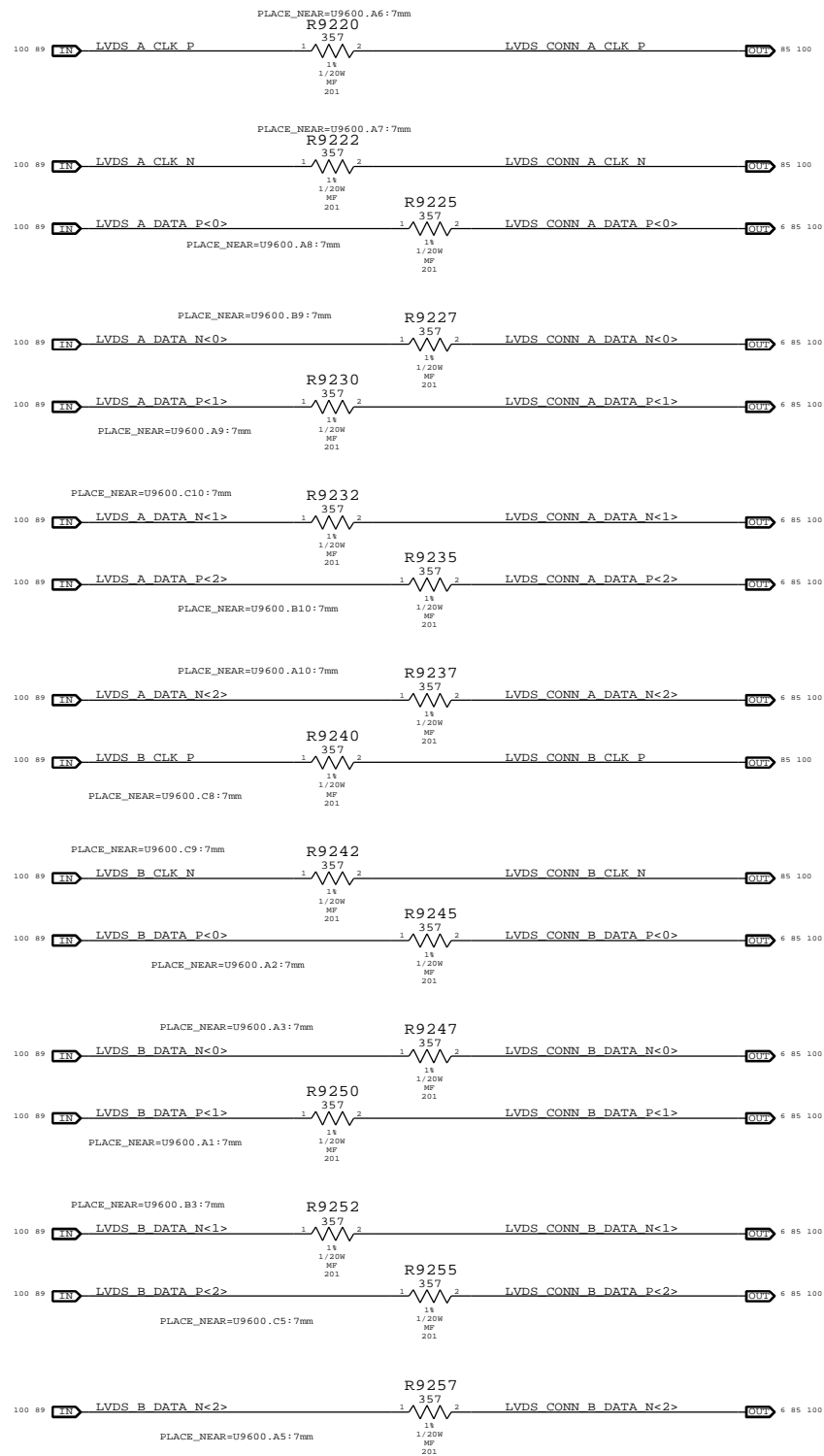
3

2

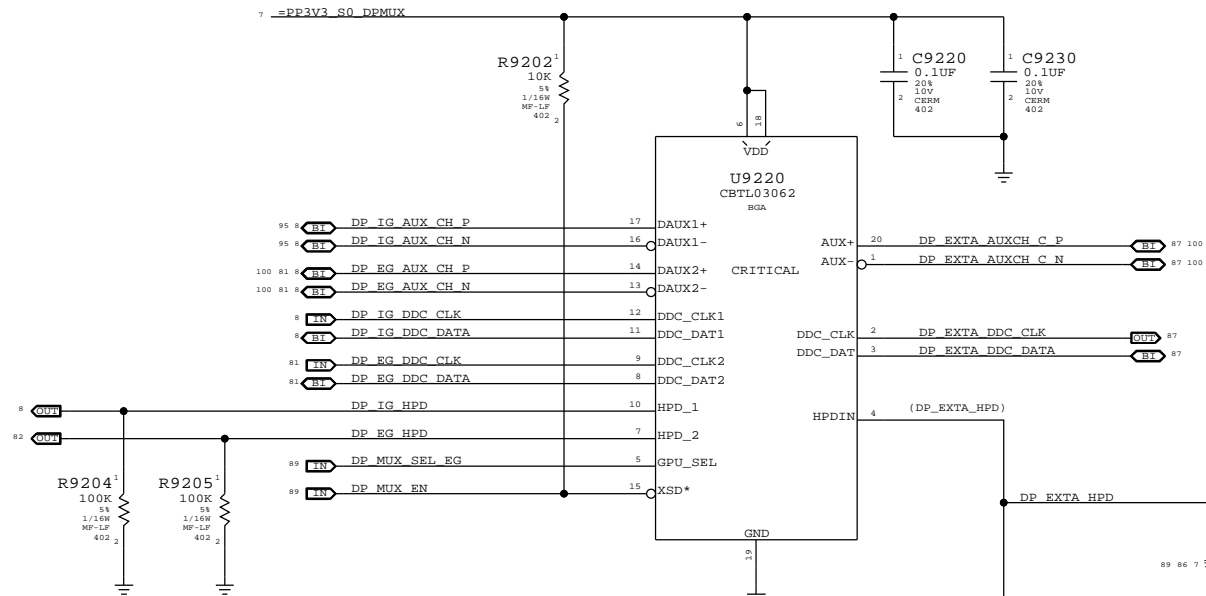
1

LVDS Transmitter Termination

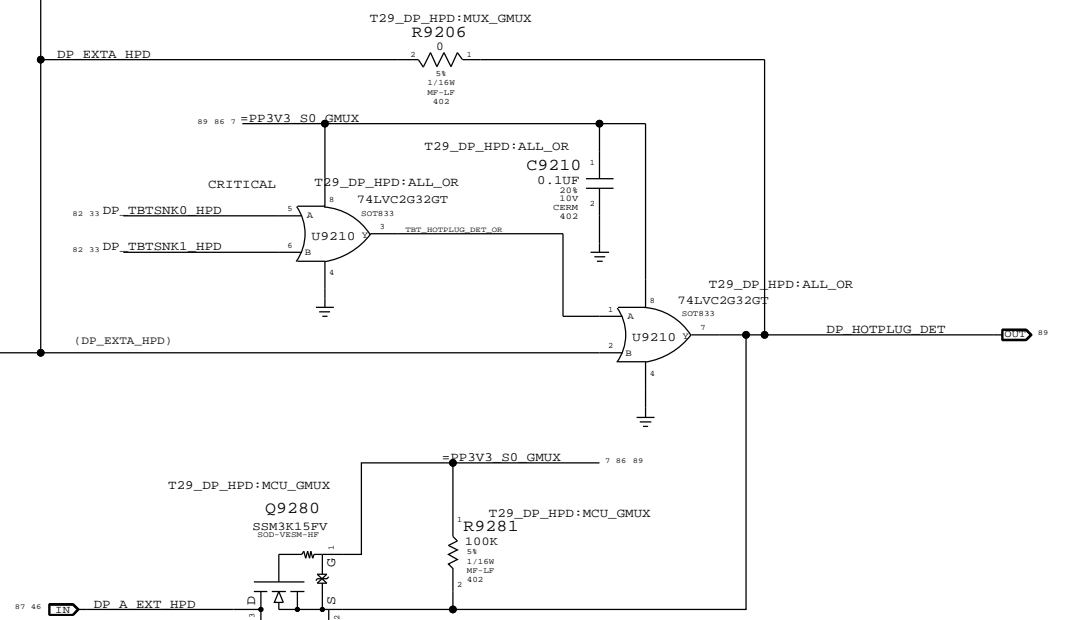
All emulated LVDS outputs require this termination



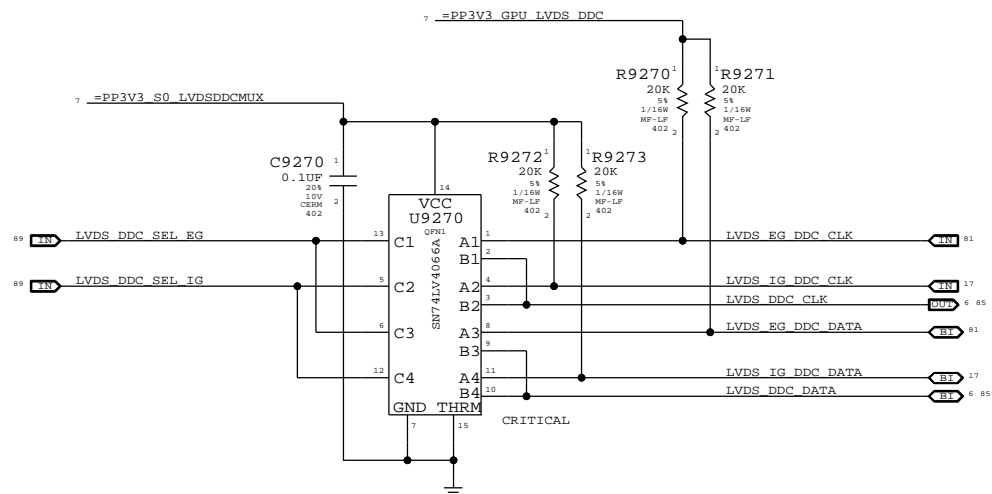
DP AUX, DDC, & HPD muxing to IG/EG



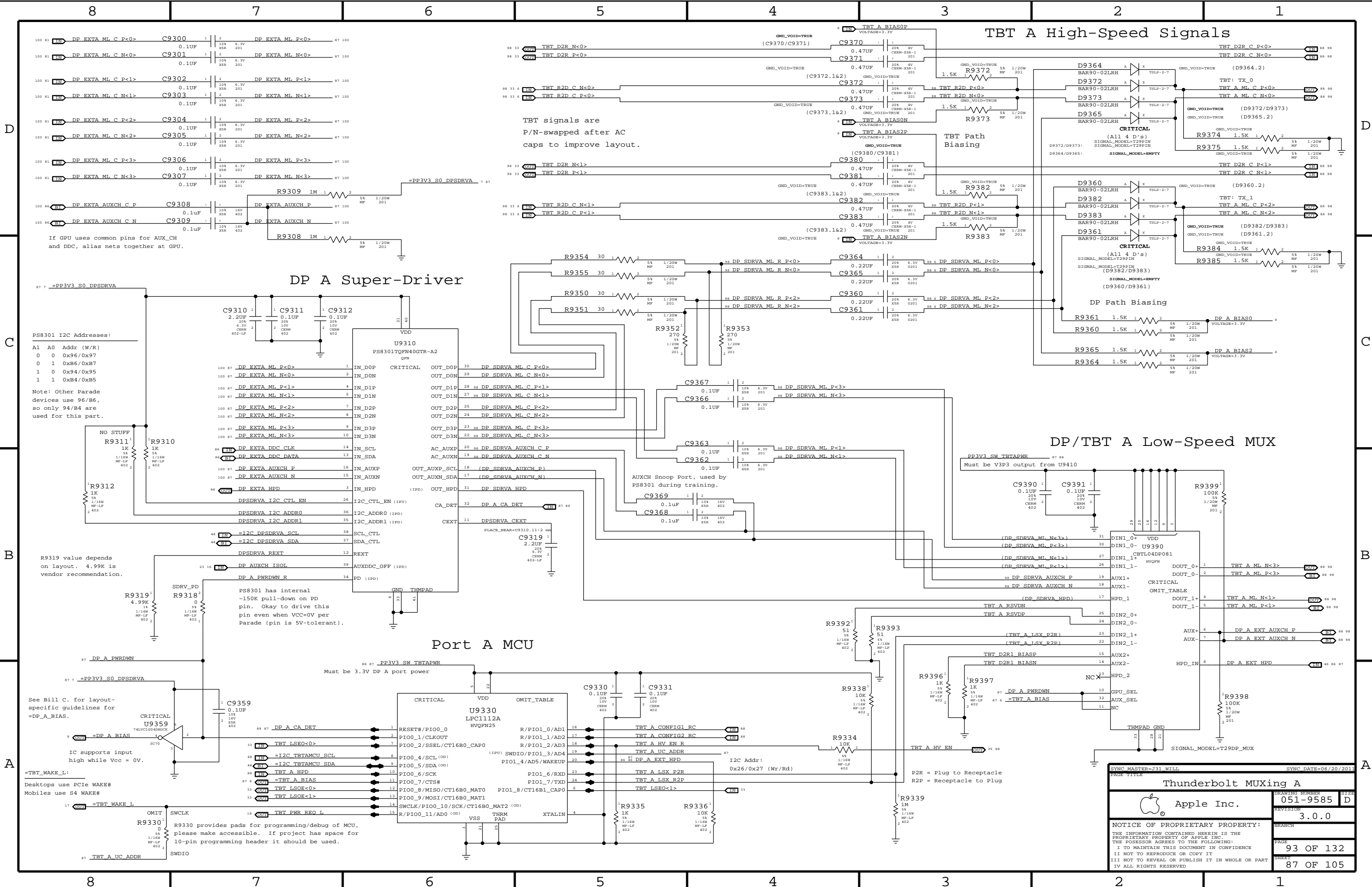
TBT/DP HOT PLUG IN



LVDS DDC MUX



SYNC MASTER=K92 MLB		SYNC DATE=11/21/2010	
PAGE TITLE		PAGE	
Muxed Graphics Support		DRAWING NUMBER	051-9585
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TBT signals are P/N-swapped after AC caps to improve layout.

TBT Path Biasing

CRITICAL

CRITICAL

DP Path Biasing

DP/TBT A Low-Speed MUX

Port A MCU

SYNC MASTER=J31 WTL

SYNC DATE=06/20/2011

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051-9585

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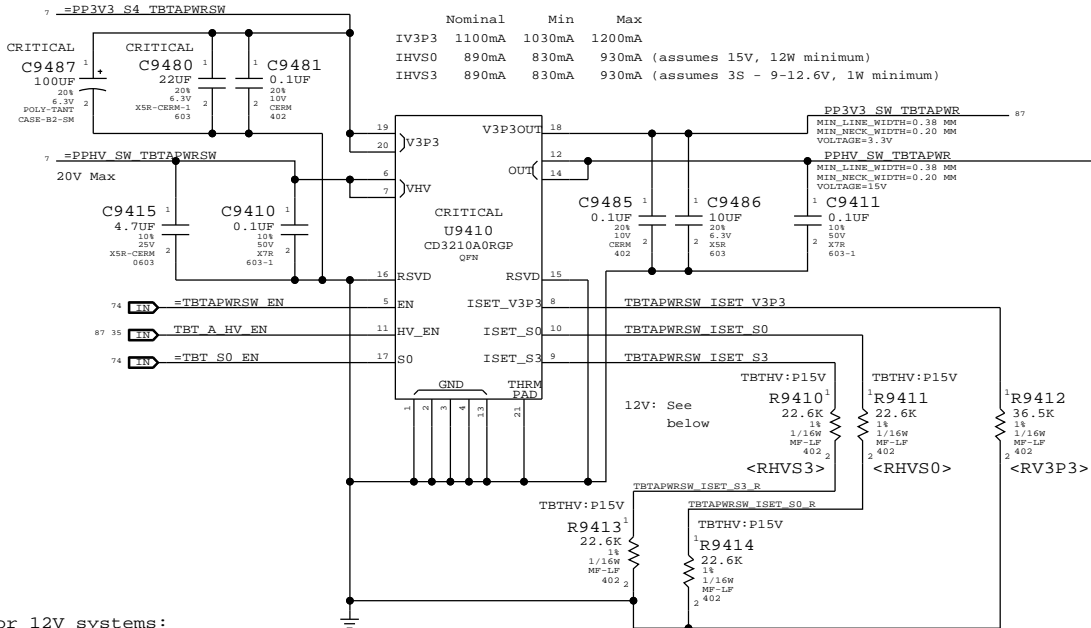
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.



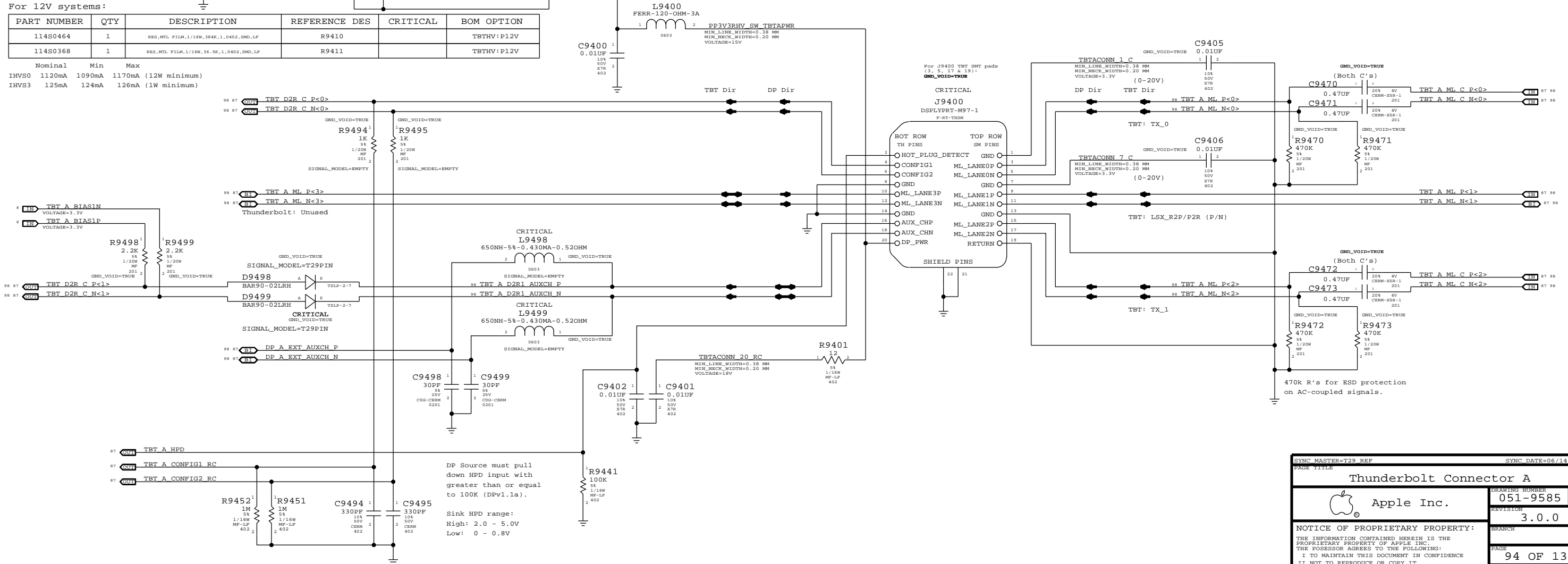
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,384K,1,0402,SMD,LF	R9410	CRITICAL	TBTHV:P12V
114S0368	1	RES,MTL FILM,1/16W,36.5K,1,0402,SMD,LF	R9411	CRITICAL	TBTHV:P12V

	Nominal	Min	Max
IHV50	1120mA	1090mA	1170mA (12W minimum)
IHV53	125mA	124mA	126mA (1W minimum)


ILIM = 40000 / R1SET

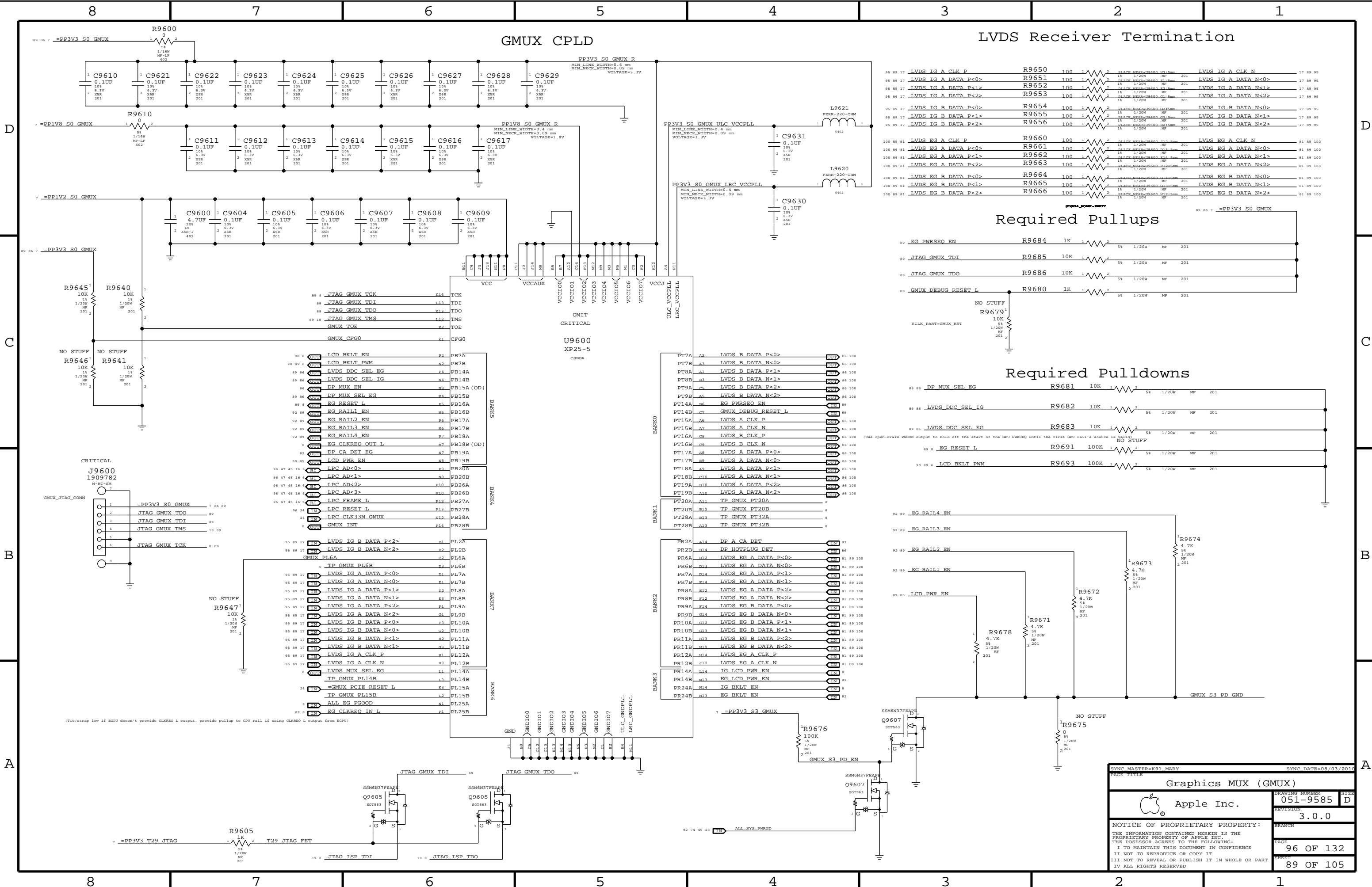
Thunderbolt Connector A



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC MASTER=T29 REF		SYNC DATE=06/14/2011	
PAGE TITLE			
Thunderbolt Connector A			
 Apple Inc.		DRAWING NUMBER	051-9585
		REVISION	3.0.0
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GMUX CPLD

LVDS Receiver Termination

Required Pullups

Required Pulldowns

SYNC MASTER=K91 MARY

SYNC DATE=08/03/2010

Graphics MUX (GMUX)

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051-9585

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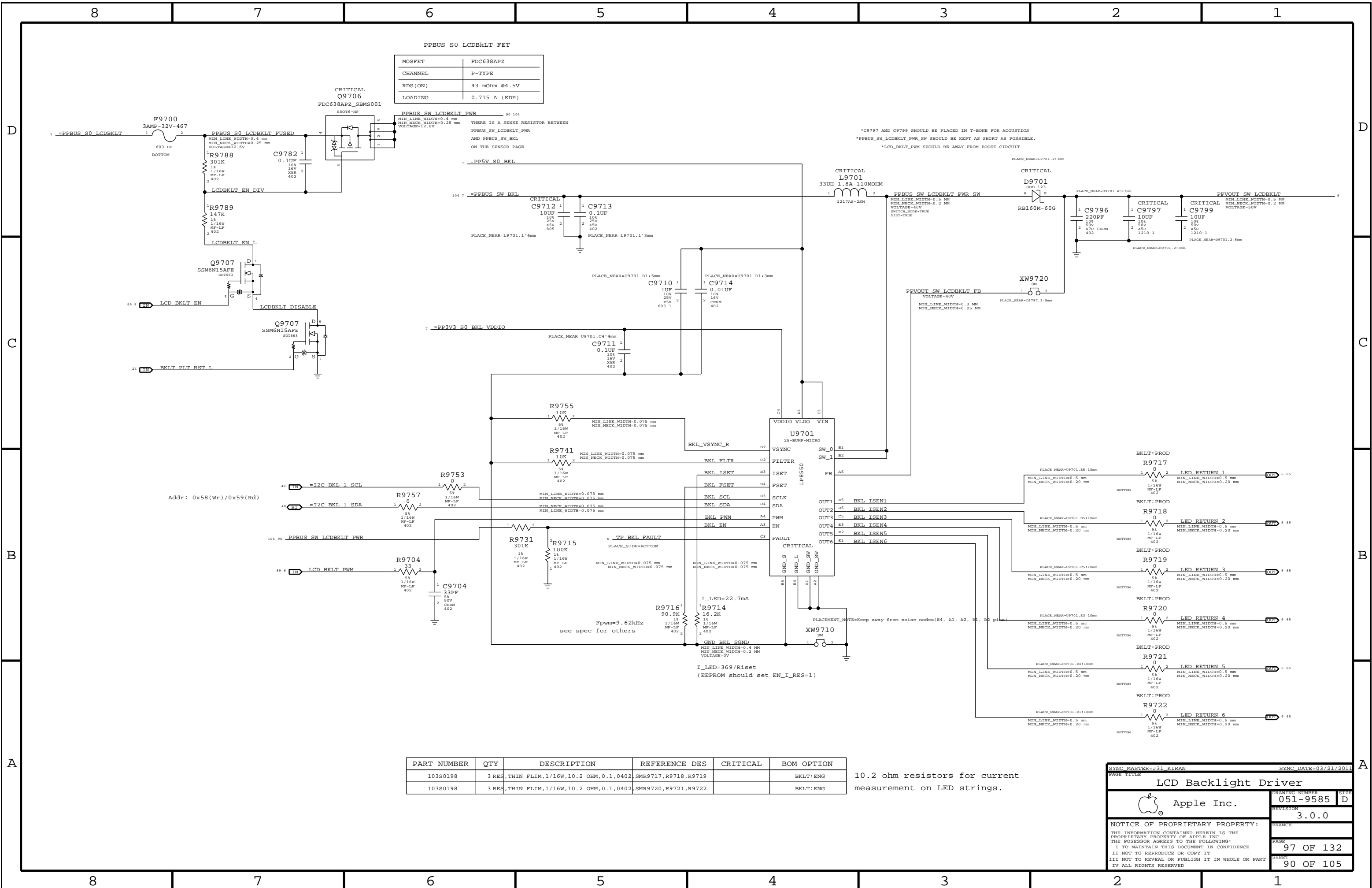
3.0.0

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
SHEET

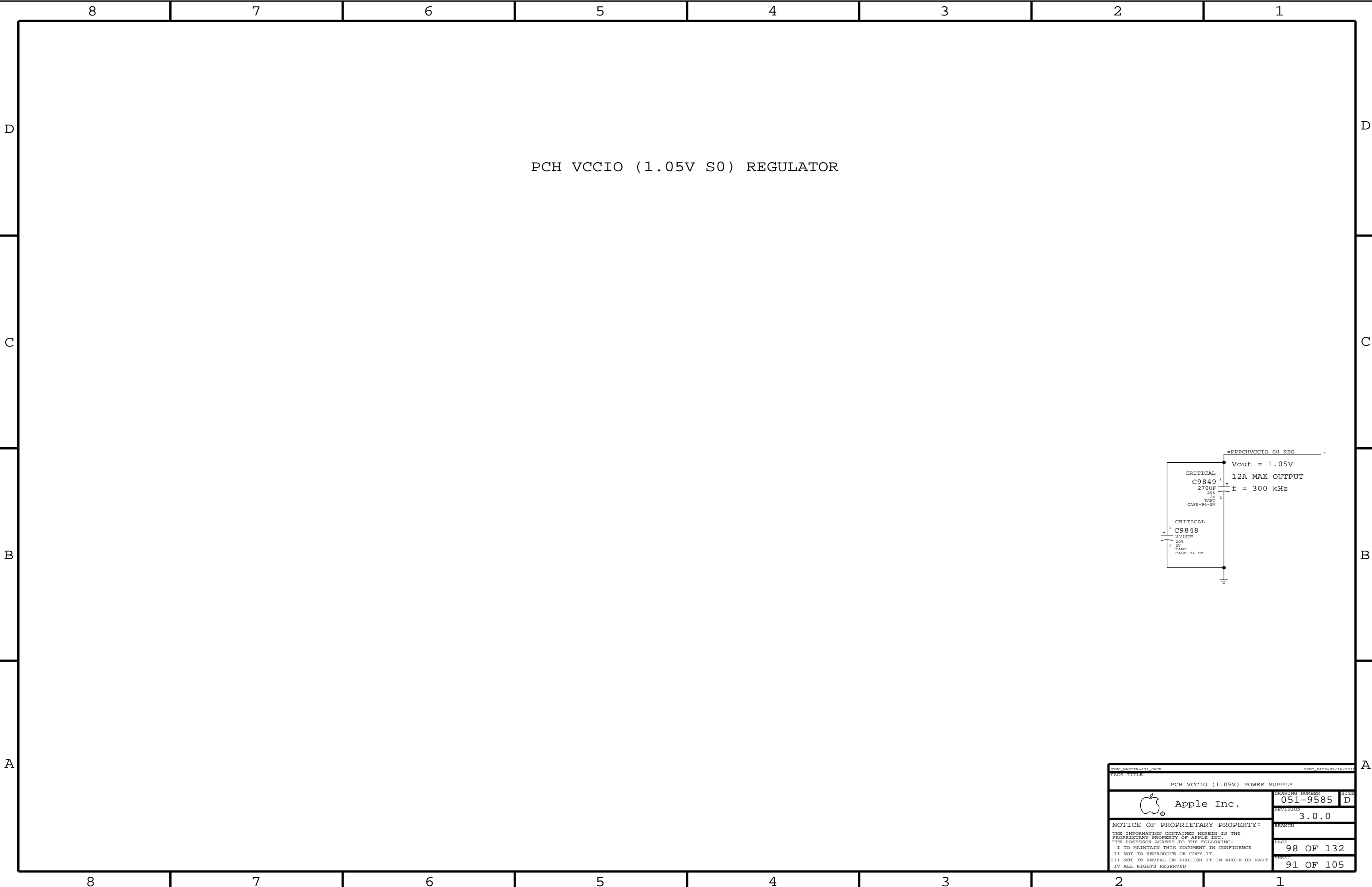
89 OF 105



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3 RES	THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0.402	SMR9717, R9718, R9719		BKLT:ENG
103S0198	3 RES	THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0.402	SMR9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=J31 KIRAN		SYNC DATE=03/21/2011	
PAGE TITLE			
LCD Backlight Driver			
 Apple Inc.		DRAWING NUMBER	051-9585
		SIZE	D
		REVISION	3.0.0
		BRANCH	
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		PAGE	97 OF 132
		SHEET	90 OF 105



PAGE TITLE		PAGE TITLE	
PCH VCCIO (1.05V) POWER SUPPLY		PCH VCCIO (1.05V) POWER SUPPLY	
DRAWING NUMBER		DRAWING NUMBER	
051-9585		051-9585	
REVISION		REVISION	
3.0.0		3.0.0	
BRANCH		BRANCH	
PAGE		PAGE	
98 OF 132		98 OF 132	
SHEET		SHEET	
91 OF 105		91 OF 105	

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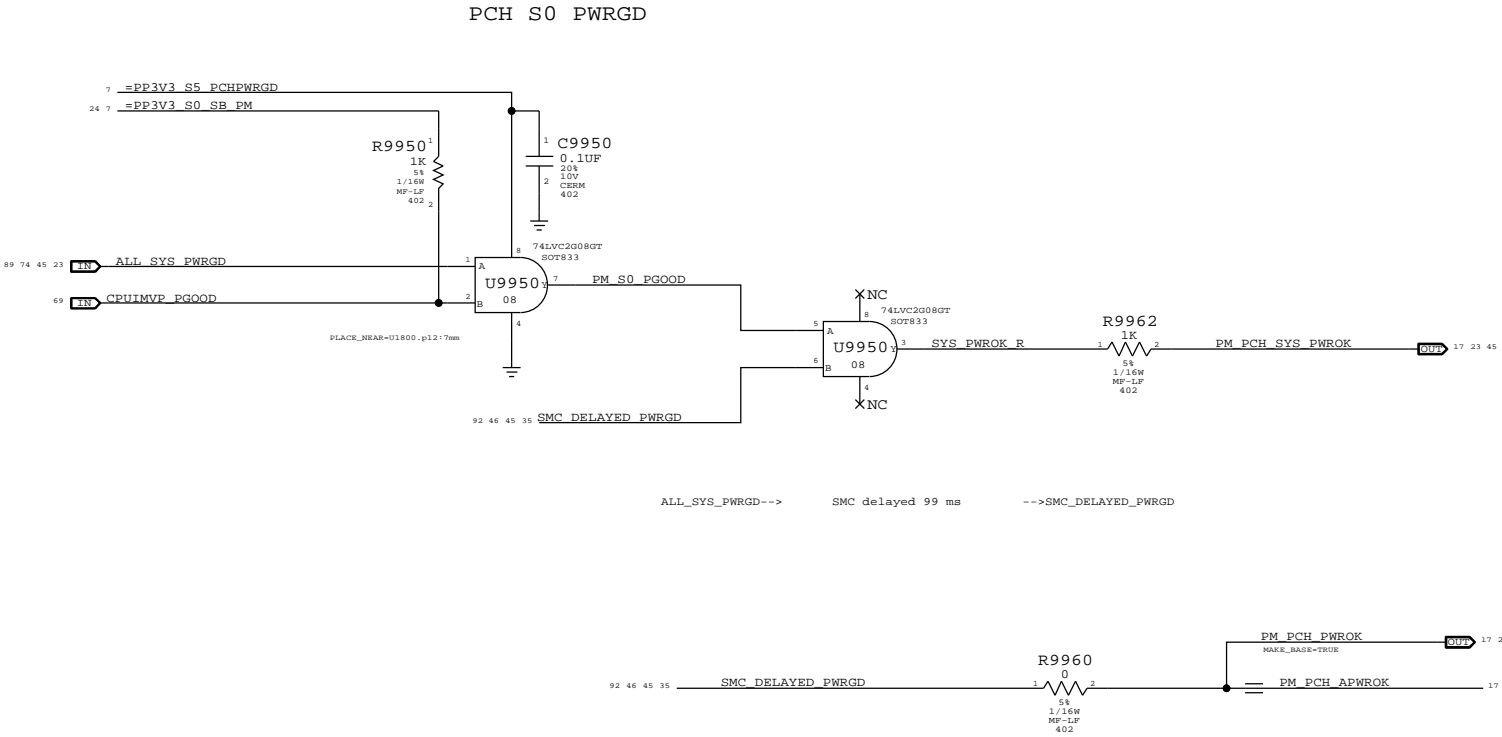
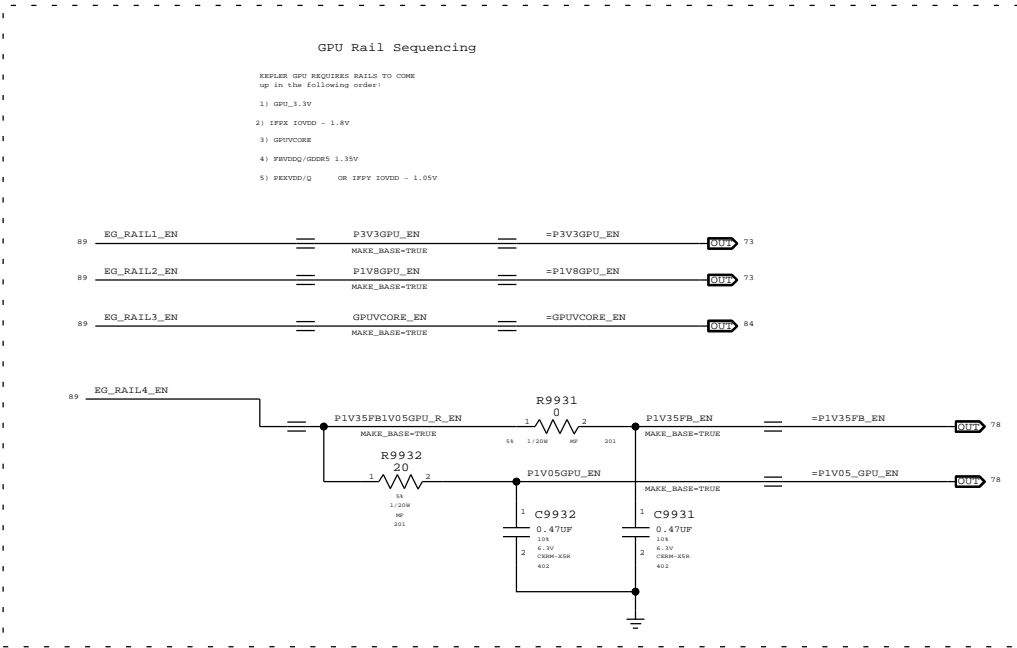
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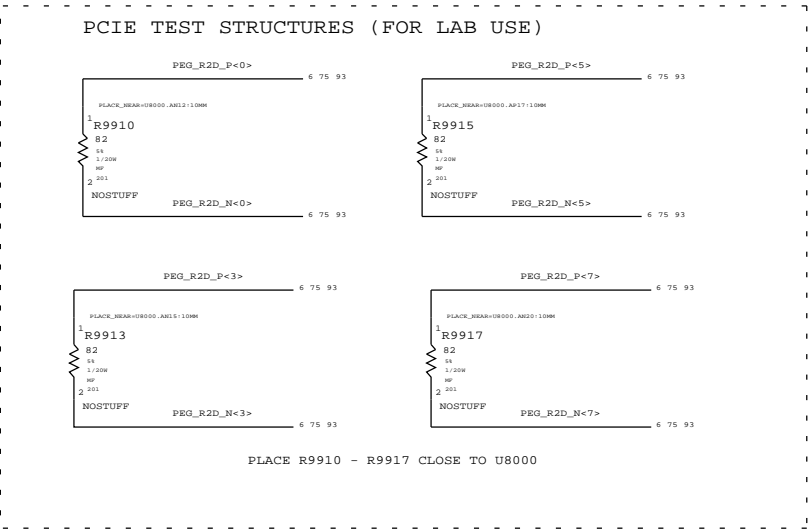
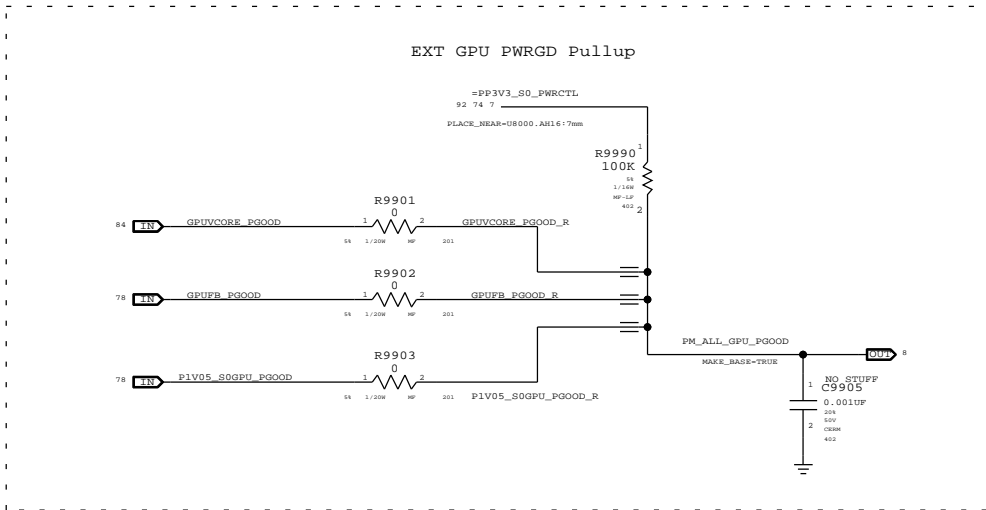
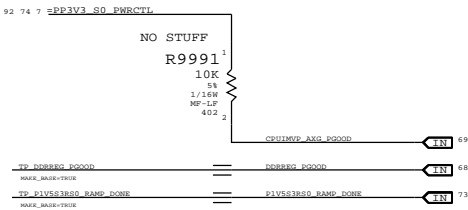
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
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Unused PGOOD signal



SYNC MASTER=J31 SREE		SYNC DATE=09/19/2011	
PAGE TITLE			
Power Sequencing EG/PCH S0			
	DRAWING NUMBER		SIZE
	051-9585		D
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2X_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?	PCIE	TOP,BOTTOM	15 MIL	?
CLK_PCIE	*	20 MIL	?				

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RRX	*	=3X_DIELECTRIC	?
PEG_TXTX	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S P<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S N<3:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA N<7:0>	6 9 17
FDI_FSYNC	CEU_50S	CEU_AGTL	FDI_FSYNC<1..0>	6 9 17
FDI_FSYNC	CEU_50S	CEU_AGTL	FDI_FSYNC<1..0>	6 9 17
FDI_INT	CEU_50S	CEU_AGTL	FDI_INT	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M CPU P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M CPU N	10 16
DP_INT	DP_85D	DISPLAYPORT	DP_INT IG ML P<3:0>	6 9
DP_INT	DP_85D	DISPLAYPORT	DP_INT IG ML N<3:0>	6 9
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT IG AUX P	6 9
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT IG AUX N	6 9
CPU_EDP_COMP	CEU_27P4S	CEU_COMP	CPU_EDP_COMP	9
CPU_PEG_COMP	CEU_27P4S	CEU_COMP	CPU_PEG_COMP	9
CPU_CFG	CEU_50S	CEU_ITP	CPU_CFG<17..0>	9 23
VDR_CLK_CEU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M P	10 16
VDR_CLK_CEU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M N	10 16
XDP_CLK_CCH	CLK_PCIE_90D	CLK_PCIE	ITEXDP_CLK100M P	16 23
XDP_CLK_CCH	CLK_PCIE_90D	CLK_PCIE	ITEXDP_CLK100M N	16 23
DPLL_REF_CLKP	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	8
DPLL_REF_CLKN	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	8
XDP_CPU_TDI	CEU_50S	CEU_ITP	XDP_CPU_TDI	10 23
VDR_TDI	CEU_50S	CEU_ITP	XDP_CPU_TDI	10 23
XDP_TMS	CEU_50S	CEU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CEU_50S	CEU_ITP	XDP_CPU_TCK	10 23
VDR_TRST_I	CEU_50S	CEU_ITP	XDP_CPU_TRST_I	10 23
XDP_BPM	CEU_50S	CEU_ITP	XDP_BPM L<3..0>	10 23
XDP_BPM_I	CEU_50S	CEU_ITP	XDP_BPM L<7..4>	10 23
VDR_DBRESET_I	CEU_50S	CEU_ITP	XDP_DBRESET_I	10 23 24
XDP_PBDY_I	CEU_50S	CEU_ITP	XDP_CPU_PBDY_I	10 23
XDP_PREQ_I	CEU_50S	CEU_ITP	XDP_CPU_PREQ_I	10 23
CPU_CATERR_I	CEU_50S	CEU_AGTL	CPU_CATERR_I	10 45
CPU_PROC_SEL_I	CEU_50S	CEU_AGTL	CPU_PROC_SEL_I	10 19
CPU_PECI	CEU_50S	CEU_VID	CPU_PECI	10 19 46
CPU_PROCHOT_I	CEU_50S	CEU_AGTL	CPU_PROCHOT_I	10 45 46 69
XDP_CPU_PWRGD	CEU_50S	CEU_ITP	XDP_CPU_PWRGD	23
PM_THERMTRIP_I	CEU_50S	CEU_8MIL	PM_THERMTRIP_I	10 19 46
PM_SYNC	CEU_50S	CEU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CEU_50S	CEU_AGTL	PM_MEM_PWRGD	10 17 26
CPU_PWRGD	CEU_50S	CEU_AGTL	CPU_PWRGD	10 19 23
CPU_SM_RCOMP	CEU_27P4S	CEU_COMP	CPU_SM_RCOMP<2..0>	10
CPU_VIDSOUT	CEU_50S	CEU_VID	CPU_VIDSOUT	12 69
CPU_VIDSCLE	CEU_50S	CEU_VID	CPU_VIDSCLE	12 69
CPU_VIDALERT_I	CEU_50S	CEU_VID	CPU_VIDALERT_I	12 69
CPU_VCCSA_VID<1..0>	CEU_50S	CEU_VID	CPU_VCCSA_VID<1..0>	12 66
CPU_VCCSENSE_P	SENSE_170I_55C	SENSE	CPU_VCCSENSE_P	12 69
CPU_VCCSENSE_N	SENSE_170I_55C	SENSE	CPU_VCCSENSE_N	12 69
CPU_VCCIOSENSE_P	SENSE_170I_55C	SENSE	CPU_VCCIOSENSE_P	12 71
CPU_VCCIOSENSE_N	SENSE_170I_55C	SENSE	CPU_VCCIOSENSE_N	12 71
CPU_AXG_SENSE_P	SENSE_170I_55C	SENSE	CPU_AXG_SENSE_P	12 69
CPU_AXG_SENSE_N	SENSE_170I_55C	SENSE	CPU_AXG_SENSE_N	12 69
CPU_VCC_VALSENSE_P	SENSE_170I_55C	SENSE	CPU_VCC_VALSENSE_P	12
CPU_VCC_VALSENSE_N	SENSE_170I_55C	SENSE	CPU_VCC_VALSENSE_N	12
CPU_AXG_VALSENSE_P	SENSE_170I_55C	SENSE	CPU_AXG_VALSENSE_P	12
CPU_AXG_VALSENSE_N	SENSE_170I_55C	SENSE	CPU_AXG_VALSENSE_N	12
CPU_VCCSASENSE	CEU_50S	CEU_AGTL	CPU_VCCSASENSE	12 66
PPCPU_MEM_VREFDQ_A	CEU_VREF	CEU_VREF	PPCPU_MEM_VREFDQ_A	9 31
PPCPU_MEM_VREFDQ_B	CEU_VREF	CEU_VREF	PPCPU_MEM_VREFDQ_B	9 31
PP0V75_S3_MEM_VREFDQ_A	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFDQ_A	27 31
PP0V75_S3_MEM_VREFDQ_B	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFDQ_B	27 31
PP0V75_S3_MEM_VREFCA_A	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFCA_A	27 31
PP0V75_S3_MEM_VREFCA_B	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFCA_B	27 31
XDP_CPU_CLK100M_P	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CPU_CLK100M_N	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
PEG_R2D P<7..0>	PEG_80D	PEG_R2D	PEG_R2D P<7..0>	6 75 92
PEG_R2D N<7..0>	PEG_80D	PEG_R2D	PEG_R2D N<7..0>	6 75 92
PEG_R2D C P<7..0>	PEG_80D	PEG_R2D	PEG_R2D C P<7..0>	8 75
PEG_R2D C N<7..0>	PEG_80D	PEG_R2D	PEG_R2D C N<7..0>	8 75
PEG_D2R P<7..0>	PEG_80D	PEG_D2R	PEG_D2R P<7..0>	8 75
PEG_D2R N<7..0>	PEG_80D	PEG_D2R	PEG_D2R N<7..0>	8 75
PEG_D2R C P<7..0>	PEG_80D	PEG_D2R	PEG_D2R C P<7..0>	6 75
PEG_D2R C N<7..0>	PEG_80D	PEG_D2R	PEG_D2R C N<7..0>	6 75

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	SDA3, SDA4, SDA5, SDA10	=4:1_SPACING	?	DISPLAYPORT	TOP, BOTTOM	=4:1_SPACING	?
LVDS	SDA3, SDA4, SDA5, SDA10	=4:1_SPACING	?	LVDS	TOP, BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D_ALT	*	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?


SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1x1+

USB 3.0 Interface Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=5:1_SPACING	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
DP_AUX_CH	DP_85D	DISPLAYPORT	DP IG AUX CH P	8	86
DP_AUX_CH	DP_85D	DISPLAYPORT	DP IG AUX CH N	8	86
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS IG A CLK P	17	89
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS IG A CLK N	17	89
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS IG A DATA P<2..0>	17	89
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS IG A DATA N<2..0>	17	89
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS IG A DATA P<3>	8	17
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS IG A DATA N<3>	8	17
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS IG B DATA P<2..0>	17	89
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS IG B DATA N<2..0>	17	89
SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA HDD R2D C P	16	41
SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA HDD R2D C N	16	41
SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA HDD R2D RC P	41	
SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA HDD R2D RC N	41	
SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA HDD R2D P	6	41
SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA HDD R2D N	6	41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA HDD D2R P	16	41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA HDD D2R N	16	41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA HDD D2R C P	6	41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA HDD D2R C N	6	41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA HDD D2R RC P	41	
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA HDD D2R RC N	41	
SATA_HDD_R2D_EDROUT	SATA_90D_ALT	SATA	SATA HDD R2D EDROUT P	41	
SATA_HDD_R2D_EDROUT	SATA_90D_ALT	SATA	SATA HDD R2D EDROUT N	41	
SATA_HDD_D2R_RDRIN	SATA_90D_ALT	SATA	SATA HDD D2R RDRIN P	41	
SATA_HDD_D2R_RDRIN	SATA_90D_ALT	SATA	SATA HDD D2R RDRIN N	41	
SATA_HDD_D2R_EDROUT	SATA_90D_ALT	SATA	SATA HDD D2R EDROUT P	41	
SATA_HDD_D2R_EDROUT	SATA_90D_ALT	SATA	SATA HDD D2R EDROUT N	41	
SATA_HDD_R2D_RDRIN	SATA_90D_ALT	SATA	SATA HDD R2D RDRIN P	41	
SATA_HDD_R2D_RDRIN	SATA_90D_ALT	SATA	SATA HDD R2D RDRIN N	41	
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P	16	41
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N	16	41
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P	6	41
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N	6	41
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P	16	41
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N	16	41
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C P	6	41
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C N	6	41
PCH_SATA3_ICOMP	SATA_50SR	SATA_ICOMP	PCH_SATA3ICOMP	16	
PCH_SATA3_ICOMP	SATA_37SR	SATA_ICOMP	PCH_SATA3ICOMP	16	
USB_EXTA	USB_85D	USB	USB_EXTA P	18	42
USB_EXTA	USB_85D	USB	USB_EXTA N	18	42
USB_EXTB_MUX	USB_85D	USB	USB_EXTB_MUX P	25	43
USB_EXTB_MUX	USB_85D	USB	USB_EXTB_MUX N	25	43
USB_EXTC	USB_85D	USB	USB_EXTC P	8	18
USB_EXTC	USB_85D	USB	USB_EXTC N	8	18
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN P	6	32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN N	6	32
USB_CAMERA	USB_85D	USB	USB_CAMERA P	18	32
USB_CAMERA	USB_85D	USB	USB_CAMERA N	18	32
USB_BT	USB_85D	USB	USB_BT P	8	32
USB_BT	USB_85D	USB	USB_BT N	8	32
USB_BT	USB_85D	USB	USB_BT_CONN P	6	32
USB_BT	USB_85D	USB	USB_BT_CONN N	6	32
USB_TPAD	USB_85D	USB	USB_TPAD P	8	53
USB_TPAD	USB_85D	USB	USB_TPAD N	8	53
USB_TPAD	USB_85D	USB	USB_TPAD R P	25	53 101
USB_TPAD	USB_85D	USB	USB_TPAD R N	25	53 101
USB_EXTD_XHCI	USB_85D	USB	USB_EXTD_XHCI P	18	25
USB_EXTD_XHCI	USB_85D	USB	USB_EXTD_XHCI N	18	25
USB_HUB_UP	USB_85D	USB	USB_HUB_UP P	18	25
USB_HUB_UP	USB_85D	USB	USB_HUB_UP N	18	25

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


SPI Interface Constraints

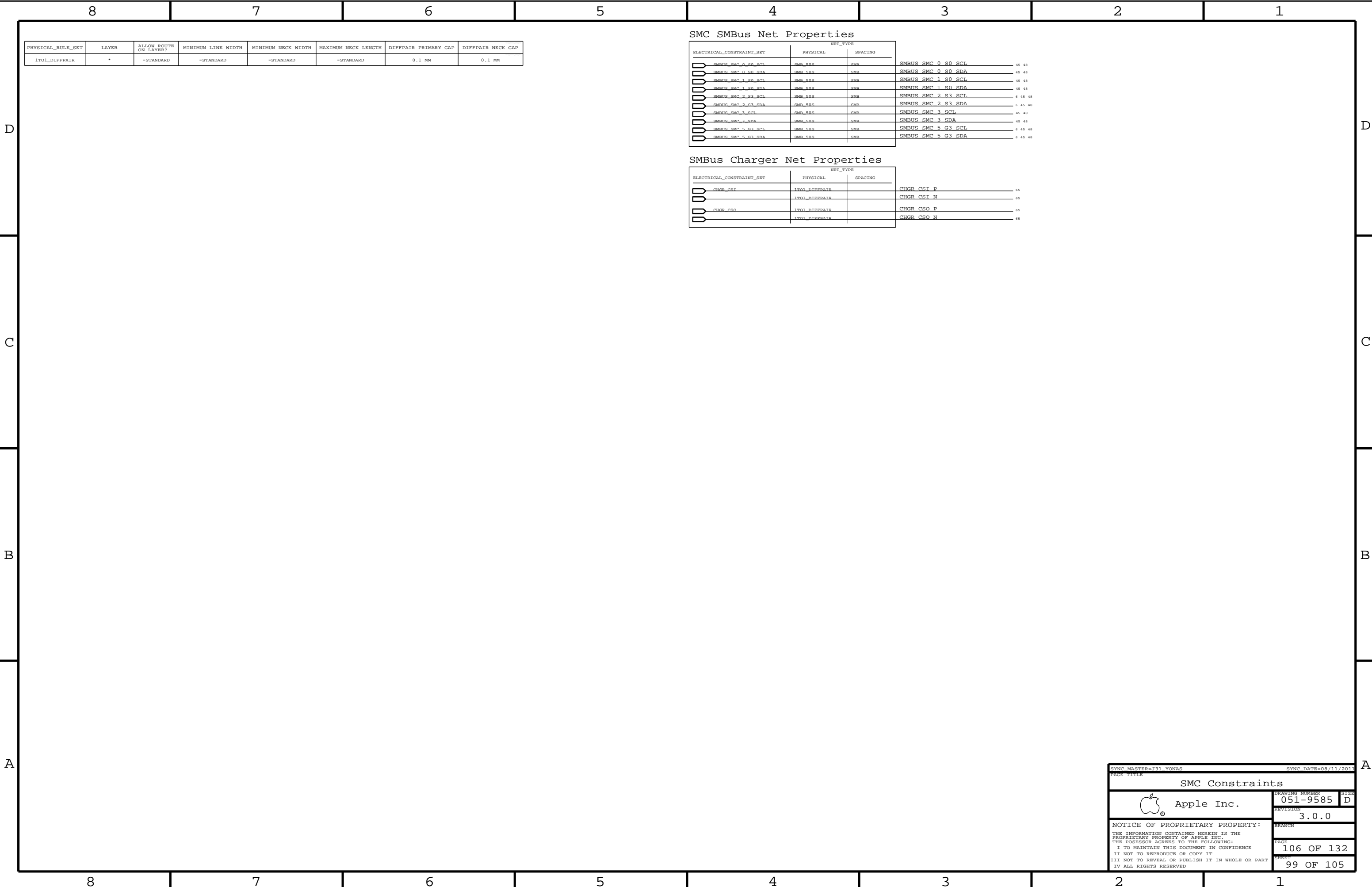
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55G	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL		NET_TYPE	SPACING	
		LPC 50R	LPC	LPC AD<3...0>		6 16 45 47 89
	LPC_FRAME_L	LPC 50R	LPC	LPC FRAME L		6 16 45 47 89
	LPC_RESET_L	LPC 50R	LPC	LPC RESET L		24 89
	RCH LPC CLK0	CLK LPC 50R	CLK LPC	LPC CLK33M SMC R		18 24
		CLK LPC 50R	CLK LPC	LPC CLK33M SMC		24 45
		CLK LPC 50R	CLK LPC	LPC CLK33M LPEPLUS		6 24 47
	SMBUS_PCH_CLK	SMB 50R	SMB	SMBUS_PCH_CLK		16 48
	SMBUS_PCH_DATA	SMB 50R	SMB	SMBUS_PCH_DATA		16 48
	SMBUS_PCH_0_CLK	SMB 50R	SMB	SML_PCH_0_CLK		16 48
	SMBUS_PCH_0_DATA	SMB 50R	SMB	SML_PCH_0_DATA		16 48
	SMBUS_PCH_1_CLK	SMB 50R	SMB	SML_PCH_1_CLK		16 48
	SMBUS_PCH_1_DATA	SMB 50R	SMB	SML_PCH_1_DATA		16 48
	HDA_BIT_CLK	HDA 50R	HDA	HDA_BIT_CLK		16 57
		HDA 50R	HDA	HDA_BIT_CLK_R		
	HDA_SYNC	HDA 50R	HDA	HDA_SYNC		16 57
		HDA 50R	HDA	HDA_SYNC_R		16
	HDA_RST_L	HDA 50R	HDA	HDA_RST_R_L		16
		HDA 50R	HDA	HDA_RST_L		16 57
	HDA_SDIN0	HDA 50R	HDA	HDA_SDIN0		16 57
		HDA 50R	HDA	AUD_SDI_R		57
	HDA_SDOUT	HDA 50R	HDA	HDA_SDOUT		16 57
		HDA 50R	HDA	HDA_SDOUT_R		16 24
	SPI_CLK	SPI 55R	SPI	SPI_CLK_R		16 47
		SPI 55R	SPI	SPI_CLK		47
	SPI_MOSI	SPI 55R	SPI	SPI_MOSI_R		16 47
		SPI 55R	SPI	SPI_MOSI		47
	SPI_MISO	SPI 55R	SPI	SPI_MISO		16 47
	SPI_CS0	SPI 55R	SPI	SPI_CS0_R_L		16 47
		SPI 55R	SPI	SPI_CS0_L		47
	PCIE_BSD	PCIE	PCIE	PCIE_ENET_R2D_P		36
	PCIE_ENET_R2D	PCIE_BSD	PCIE	PCIE_ENET_R2D_N		36
		PCIE_BSD	PCIE	PCIE_ENET_R2D_C_P		16 36
		PCIE_BSD	PCIE	PCIE_ENET_R2D_C_N		16 36
	PCIE_ENET_D2R	PCIE_BSD	PCIE	PCIE_ENET_D2R_P		16 36
		PCIE_BSD	PCIE	PCIE_ENET_D2R_N		16 36
		PCIE_BSD	PCIE	PCIE_ENET_D2R_C_P		36
		PCIE_BSD	PCIE	PCIE_ENET_D2R_C_N		36
	PCIE_AP_BSD	PCIE	PCIE	PCIE_AP_R2D_P		6 32
		PCIE_BSD	PCIE	PCIE_AP_R2D_N		6 32
	PCIE_AP_R2D	PCIE_BSD	PCIE	PCIE_AP_R2D_C_P		16 32
		PCIE_BSD	PCIE	PCIE_AP_R2D_C_N		16 32
	PCIE_AP_D2R	PCIE_BSD	PCIE	PCIE_AP_D2R_P		16 32
		PCIE_BSD	PCIE	PCIE_AP_D2R_N		16 32
		PCIE_BSD	PCIE	PCIE_AP_D2R_R_P		32
		PCIE_BSD	PCIE	PCIE_AP_D2R_R_N		32
	PCIE_BSD	PCIE	PCIE	PCIE_FW_R2D_P		38
	PCIE_BSD	PCIE	PCIE	PCIE_FW_R2D_N		38
	PCIE_FW_R2D	PCIE_BSD	PCIE	PCIE_FW_R2D_C_P		16 38
		PCIE_BSD	PCIE	PCIE_FW_R2D_C_N		16 38
	PCIE_FW_D2R	PCIE_BSD	PCIE	PCIE_FW_D2R_P		16 38
		PCIE_BSD	PCIE	PCIE_FW_D2R_N		16 38
		PCIE_BSD	PCIE	PCIE_FW_D2R_C_P		38
		PCIE_BSD	PCIE	PCIE_FW_D2R_C_N		38
	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCIE_CLK100M_PCH_P		16
	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCIE_CLK100M_PCH_N		16
	PCIE_CLK100M_T2R	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P		16 33
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N		16 33
		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P		16
		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N		16
	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH_CLK100M_SATA_P		16
	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH_CLK100M_SATA_N		16
	CHU_50R	CLK_PCIE	CLK_PCIE	PCIE_CLK14P3M_REFCLK		16
	CHU_50R	CLK_PCIE	CLK_PCIE	PCH_CLK33M_PCIIN		16 24
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEX_TSTCLK_O_P		75
		CLK_PCIE_90D	CLK_PCIE	PEX_TSTCLK_O_N		75
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P		16 75
		CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N		16 75
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P		16 36
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N		16 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P		16 32
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N		16 32
	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P		16 38
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N		16 38
	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P		6 16
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N		6 16
	PCIE_T2R_R2D	PCIE_BSD	PCIE	PCIE_TBT_R2D_C_P<3...0>		6 33
	PCIE_T2R_R2D	PCIE_BSD	PCIE	PCIE_TBT_R2D_C_N<3...0>		6 33
	PCIE_T2R_D2R	PCIE_BSD	PCIE	PCIE_TBT_D2R_P<3...0>		6 33
	PCIE_T2R_D2R	PCIE_BSD	PCIE	PCIE_TBT_D2R_N<3...0>		6 33
	PCIE_T2R_R2D	PCIE_BSD	PCIE	PCIE_TBT_R2D_P<3...0>		33
	PCIE_T2R_R2D	PCIE_BSD	PCIE	PCIE_TBT_R2D_N<3...0>		33
	PCIE_T2R_D2R	PCIE_BSD	PCIE	PCIE_TBT_D2R_C_P<3...0>		33
	PCIE_T2R_D2R	PCIE_BSD	PCIE	PCIE_TBT_D2R_C_N<3...0>		33

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1701_550	*	<1:1_DIFFPAIR	>55_0HM_SE	>55_0HM_SE	>55_0HM_SE	<1:1_DIFFPAIR	<1:1_DIFFPAIR
THERM_1701_550	*	<1:1_DIFFPAIR	>55_0HM_SE	>55_0HM_SE	>55_0HM_SE	<1:1_DIFFPAIR	<1:1_DIFFPAIR
DIFFPAIR	*	<1:1_DIFFPAIR	>1:1_DIFFPAIR	>1:1_DIFFPAIR	>1:1_DIFFPAIR	<1:1_DIFFPAIR	<1:1_DIFFPAIR
AUDIODIFF	*	<1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	-2:1_SPACING	?
THERM	*	-2:1_SPACING	?
AUDIO	*	-2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
KINETCOM	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	-STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P2996
MEM_CND	QND	*	QND_P2996
MEM_CTL	QND	*	QND_P2996
MEM_FQS	QND	*	QND_P2996

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	+	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2046
PCIE	GND	*	GND_P2046
SATA	GND	*	GND_P2046
USB	GND	*	GND_P2046
CLK_PCIE	SB_POWER	*	PWR_P2046
SATA	SB_POWER	*	PWR_P2046
USB	SB_POWER	*	PWR_P2046

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVD5	GND	+	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27F4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

Physical Rule Set		
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DF_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

J31 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYICAL		SPAC	NET_TYPE	
		SENSE_1000		SENSECONN	ENETCONN P<3...0>	37
		SENSE_1000		SENSECONN	ENETCONN N<3...0>	37
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUTHMSENS D2_P	51
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUTHMSENS D2_N	51
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUTHMSENS D1_P	51
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUTHMSENS D1_N	51
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUTHMSENS D_P	51
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUTHMSENS D_N	51
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPU_TDIODE_P	51 81
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPU_TDIODE_N	51 81
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPUVCCORE SENSE_P	83 84
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPUVCCORE SENSE_N	83 84
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	VCCSASO_CS_P	49 66
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	VCCSASO_CS_N	49 66
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_1V5_S3_DDR_P	49
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_1V5_S3_DDR_N	49
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUVCCIO00_CS_P	49 71
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUVCCIO00_CS_N	49 71
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP6_CS_R_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP6_CS_R_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP6_CS_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP6_CS_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_AIRPORT_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_AIRPORT_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HDD_N	41 103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HDD_P	41 103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_LCDBKLT_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_LCDBKLT_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP_ISNS2_P	84
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP_ISNS2_N	84
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V0_S0GPU_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V0_S0GPU_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V5_S3_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V5_S3_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP_ISNS1_P	84
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GFXIMVP_ISNS1_N	84
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V05_S0GPU_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V05_S0GPU_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP3V3_S0GPU_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP3V3_S0GPU_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_TBT_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_TBT_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNSIG_P	50 70
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNSIG_N	50 70
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNSIG_R_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNSIG_R_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS20_P	50 70
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS20_N	50 70
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS1_P	50 69
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS1_N	50 69
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS2_P	50 69
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS2_N	50 70
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS3_P	50 69
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS3_N	50 70
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HS_OTHER_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HS_OTHER_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HS_GPU_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HS_GPU_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HS_COMPUTING_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_HS_COMPUTING_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISNS_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V0_S0GPU_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V0_S0GPU_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP3V3_S3_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP3V3_S3_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPU_VCORE_RMC_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPU_VCORE_RMC_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V5_S3_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V5_S3_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_GPU_R_P	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_GPU_R_N	
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_CPUVCCSA_R_P	49
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_CPUVCCSA_R_N	49
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_CPUVCCIO_R_P	49
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_CPUVCCIO_R_N	49
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISUM_R_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISUM_R_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISUMG_R_P	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	CPUMVMP_ISUMG_R_N	50
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V5_S3_R_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP1V5_S3_R_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP0PUFB_S0_R_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_PP0PUFB_S0_R_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	PIV05_GPU_CS_P	78 103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	PIV05_GPU_CS_N	78 103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPUFB_CS_P	78 103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPUFB_CS_N	78 103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_AIRPORT_R_P	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_AIRPORT_R_N	103
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_TBT_R_P	104
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	ISNS_TBT_R_N	104
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	PIV05_GPU_PEX_I0VDD_SNS_P	78 83
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	PIV05_GPU_PEX_I0VDD_SNS_N	78 83
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPU_FBVDD0_SENSE_P	77 78
	SENSE_OVERFLOW	SENSE_1000_550		SENSE	GPU_FBVDD0_SENSE_N	77 78

J31 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	SMT_TYPE
PCIE CLK100M AP	CLK_PCIE_S00	CLK_PCIE	PCIE CLK100M AP CONN P
PCIE CLK100M AP CONN N	CLK_PCIE_S00	CLK_PCIE	PCIE CLK100M AP CONN N
1T01 DIFFEAIR			CHGR CSI_R_P
1T01 DIFFEAIR			CHGR CSI_R_N
1T01 DIFFEAIR			CHGR CSO_R_P
1T01 DIFFEAIR			CHGR CSO_R_N
BT_MIC_P			BT_MIC_P
BT_MIC_N			BT_MIC_N
AUD_L01_L_P			AUD_L01_L_P
AUD_L01_L_N			AUD_L01_L_N
AUD_L01_R_P			AUD_L01_R_P
AUD_L01_R_N			AUD_L01_R_N
AUD_L02_L_P			AUD_L02_L_P
AUD_L02_L_N			AUD_L02_L_N
AUD_L02_R_P			AUD_L02_R_P
AUD_L02_R_N			AUD_L02_R_N
AUD_SPKRAMP_LIN_P			AUD_SPKRAMP_LIN_P
AUD_SPKRAMP_LIN_N			AUD_SPKRAMP_LIN_N
AUD_SPKRAMP_RIN_P			AUD_SPKRAMP_RIN_P
AUD_SPKRAMP_RIN_N			AUD_SPKRAMP_RIN_N
AUD_SPKRAMP_SUBIN_P			AUD_SPKRAMP_SUBIN_P
AUD_SPKRAMP_SUBIN_N			AUD_SPKRAMP_SUBIN_N
SSM2375S_P			SSM2375S_P
SSM2375S_N			SSM2375S_N
SSM2375S_P			SSM2375S_P
SSM2375S_N			SSM2375S_N
SSM2375S_P			SSM2375S_P
SSM2375S_N			SSM2375S_N
SPK_OUT			SPKRCONN_L_OUT_P
SPK_OUT			SPKRCONN_L_OUT_N
SPK_OUT			SPKRCONN_R_OUT_P
SPK_OUT			SPKRCONN_R_OUT_N
SPK_OUT			SPKRCONN_S_OUT_P
SPK_OUT			SPKRCONN_S_OUT_N
USB_TP4D_R_P			USB_TP4D_R_P
USB_TP4D_R_N			USB_TP4D_R_N
PP3V3_R5			PP3V3_R5
PP3V3_R0			PP3V3_R0
PP1V5_R3R50			PP1V5_R3R50
GND			GND

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J31 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, INL2, INL3, INL4, INL5, INL6, INL7, INL8, INL9, INL10, INL11, BOTTOM	NO_TYPE_BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	-50_OBM_SE	-50_OBM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	-DEFAULT	-DEFAULT	10 MM	-DEFAULT	-DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_00M_SX	TOP_BOTTOM	Y	0.090 MM	0.090 MM			
55_00M_SX	*	Y	0.076 MM	0.076 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP_BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	<STANDARD	<STANDARD	<STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_09M_SE	TOP_BOTTOM	Y	0.13 MM	0.13 MM			
45_09M_SE	*	Y	0.099 MM	0.099 MM	<STANDARD	<STANDARD	<STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP_BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_08M_SE	TOP_BOTTOM	Y	0.185 MM	0.095 MM			
37_08M_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
2704_OBM_SE	TOP_BOTTOM	Y	0.310 MM	0.095 MM			
2704_OBM_SE	*	Y	0.250 MM	0.1 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
72_OHM_DIFF	ISL1, ISL2, ISL3, ISL12	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP_BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
80_OHM_DIFF	0001, 1000, 1001, 1010	Y	0.105 MM	0.091 MM		0.120 MM	0.080 MM
80_OHM_DIFF	1011, 1011	Y	0.105 MM	0.091 MM		0.120 MM	0.080 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_08M_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
85_08M_DIFF	08L, 180L, 180L, 180L, 180L	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_08M_DIFF	ISL2, ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_08M_DIFF	TOP, BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_0MM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
90_0MM_DIFF	0ML1, 10ML, 10ML10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_0MM_DIFF	1SL2, 1SL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_0MM_DIFF	TOP_BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
100_OHM_DIFF	ISL1, ISL2, ISL3, ISL12	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP_BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
110_OHM_DIFF	10A, 10B, 10C, 10L10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	10L2, 10L11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	-DEFAULT	?
HGA_F1MM	*	-DEFAULT	?
HGA_F2MM	*	-DEFAULT	?
POT2_SPACE	*	0.071 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	-STANDARD	-STANDARD	-STANDARD	0.1 MM	0.1 MM


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF_ALT	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
90_OHM_DIFF_ALT	ISL1, ISL4, ISL5, ISL10	Y	0.099 MM	0.099 MM		0.280 MM	0.280 MM
90_OHM_DIFF_ALT	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.280 MM	0.280 MM
90_OHM_DIFF_ALT	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.300 MM	0.300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

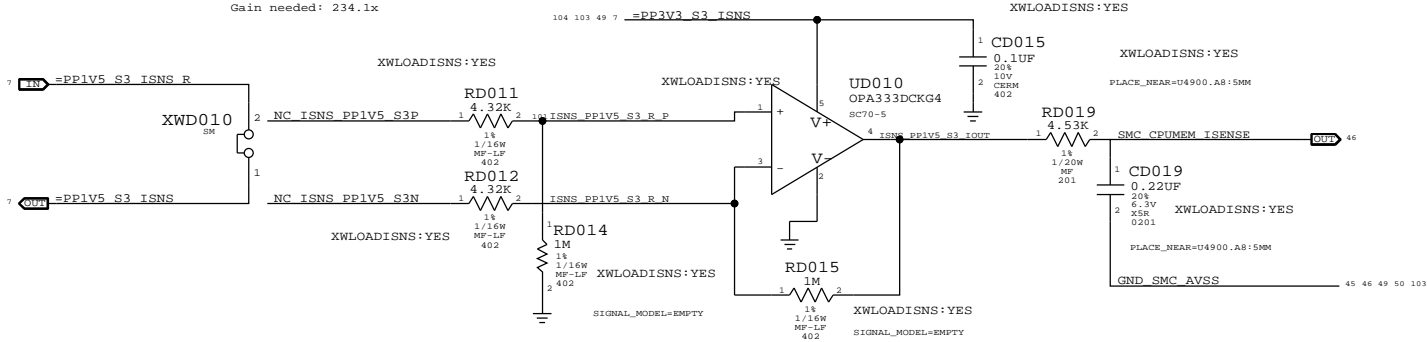
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?
10X_DIELECTRIC	*	0.700 MM	?

SYNCH MASTER-K18 MLR		SYNCH DATE=04/27/2010	
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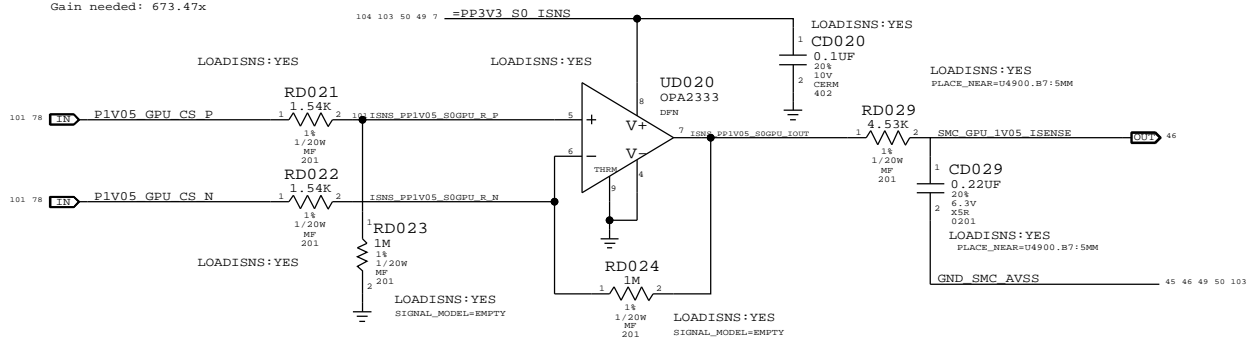
DDR 1.5V S3 (CPU & Memory) Current Sense (IM1C)

Gain: 231.4x, EDP: 14.1 A
Rsense: 0.001 (RD010)
V accross Rsense: 14.1 mV
Gain needed: 234.1x



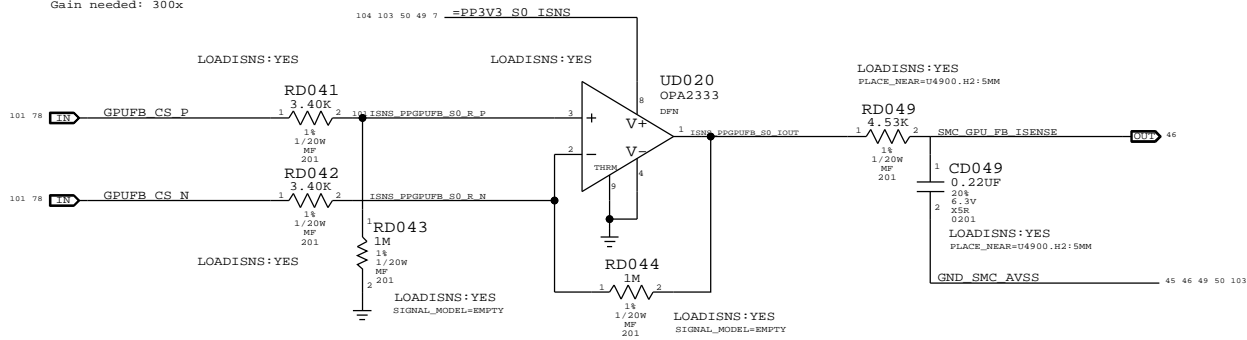
GPU 1.05V Current Sense (IG1C)

Gain: 649.35x, EDP: 4.9 A
Rsense: 0.001 (RD8310)
V accross Rsense: 4.9 mV
Gain needed: 673.47x

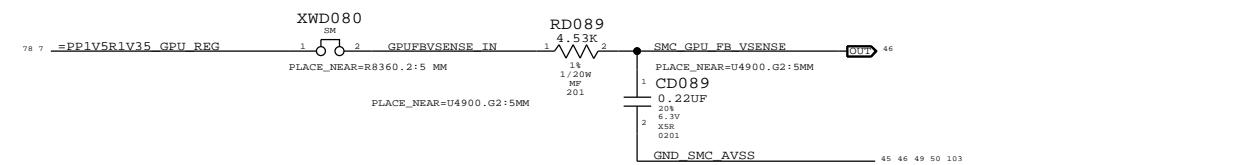


GPU FB (1.35V/1.5V) Current Sense (IG3C)

Gain: 294.12x, EDP: 11 A
Rsense: 0.001 (R8360)
V accross Rsense: 11 mV
Gain needed: 300x

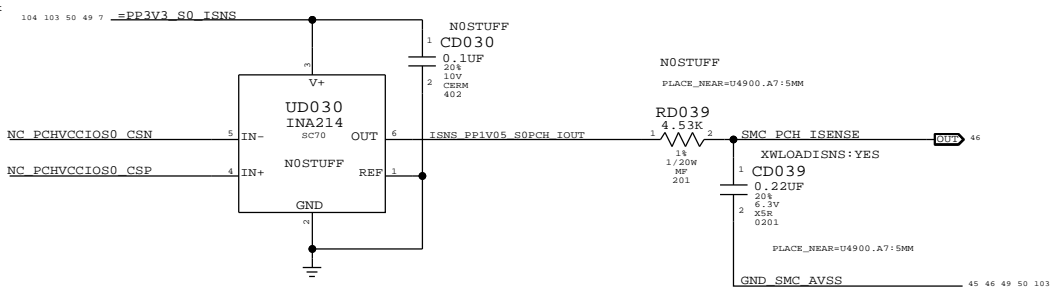


GPU FB (1.35V/1.5V) Voltage Sense (VG3C)



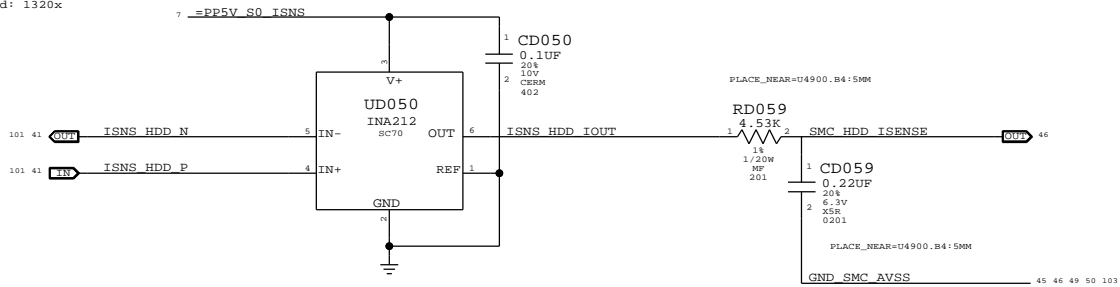
PCH Core (PCH VCCIO) Current Sense (ISBC)

Gain: 100x, EDP: 11.4 A
Rsense: 0.002 (R9840)
V accross Rsense: 22.8 mV
Gain needed: 144.7x



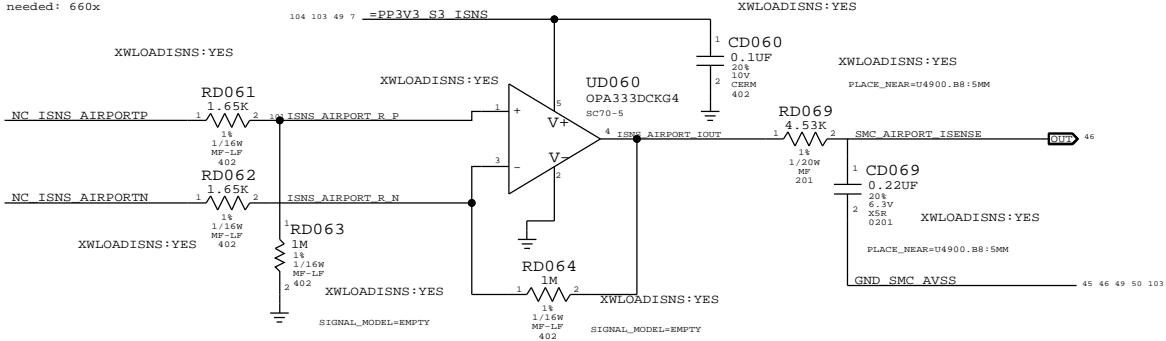
HDD Current Sense (IHDC)

Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R4599)
V accross Rsense: 2.5 mV
Gain needed: 1320x



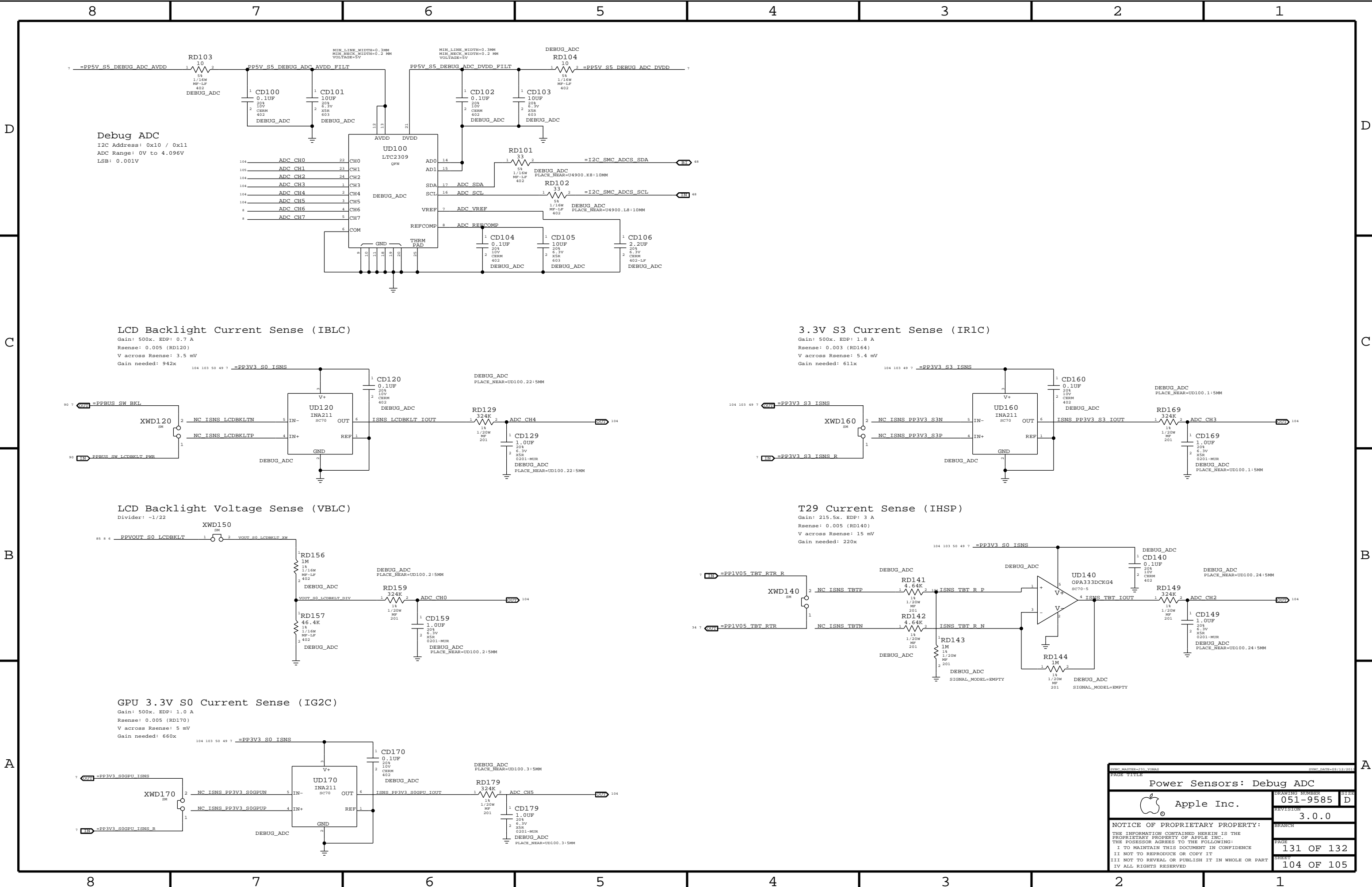
Airport Current Sense (IAPC)

Gain: 606x, EDP: 1 A
Rsense: 0.005 (R3552)
V accross Rsense: 5 mV
Gain needed: 660x



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,100K,201	CD029,CD049		LOADISNS:NO
117S0008	3	RES,100K,201	CD019,CD039,CD069		XWLOADISNS:NO

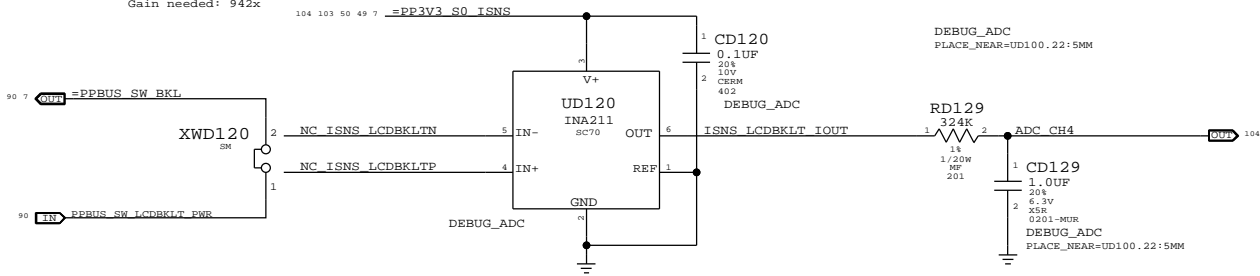
SYNC MASTER:131 YONAS		SYNC DATE:09/12/2013	
PAGE TITLE		Power Sensors: SMC Extended	
Apple Inc.		DRAWING NUMBER	051-9585
		REVISION	3.0.0
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Debug ADC
I2C Address: 0x10 / 0x11
ADC Range: 0V to 4.096V
LSB: 0.001V

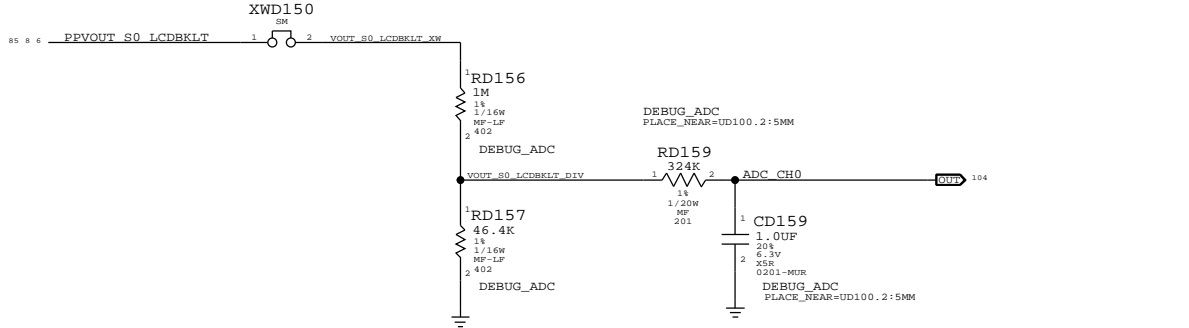
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.7 A
Rsense: 0.005 (RD120)
V across Rsense: 3.5 mV
Gain needed: 942x



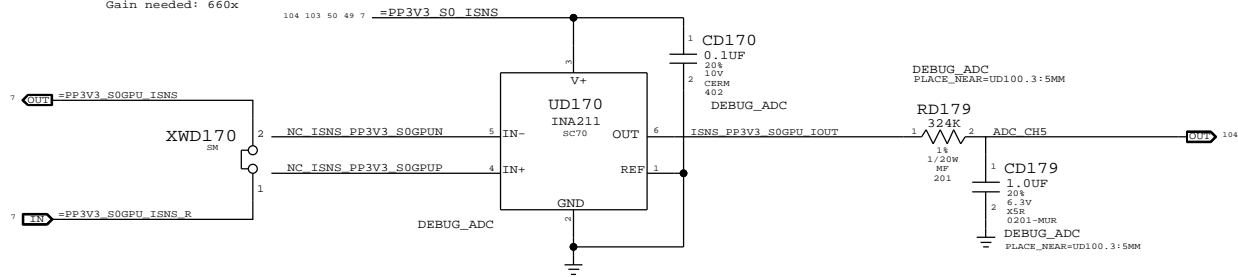
LCD Backlight Voltage Sense (VBLC)

Divider: ~1/22



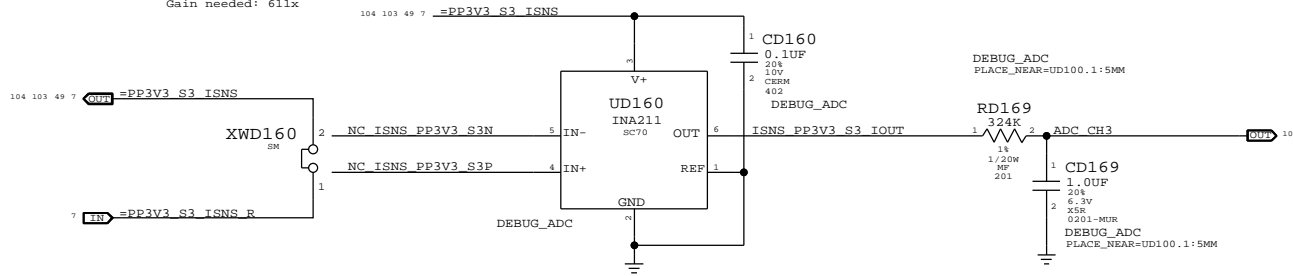
GPU 3.3V S0 Current Sense (IG2C)

Gain: 500x. EDP: 1.0 A
Rsense: 0.005 (RD170)
V across Rsense: 5 mV
Gain needed: 660x



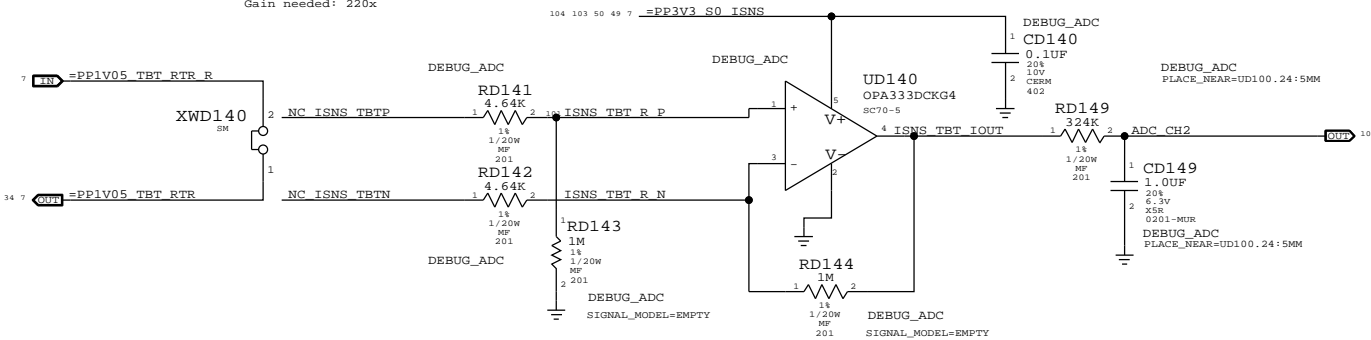
3.3V S3 Current Sense (IR1C)

Gain: 500x. EDP: 1.8 A
Rsense: 0.003 (RD164)
V across Rsense: 5.4 mV
Gain needed: 611x



T29 Current Sense (IHSP)

Gain: 215.5x. EDP: 3 A
Rsense: 0.005 (RD140)
V across Rsense: 15 mV
Gain needed: 220x



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